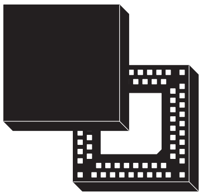
L6751C

Digitally controlled dual PWM for Intel VR12 and AMD SVI

Datasheet - production data


WPLGA72 6 x 6 mm

Features

- VR12 compliant with 25 MHz SVID bus rev. 1.5
  - SerialVID with programmable IMAX, TMAX, VBOOT, ADDRESS
- AMD SVI compliant
- Second generation LTB Technology™
- Flexible driver/DrMOS support
- JMode support
- Fully configurable through PMBus™
- Dual controller:
  - Up to 6 phases for CORE and memory
  - 1 phase for graphics (GFX), system agent (VSA) or Northbridge (VDDNB)
- Single NTC design for TM, LL and IMON thermal compensation (for each section)
- VFDE and GDC - gate drive control for efficiency optimization
- DPM - dynamic phase management
- Dual remote sense; 0.5% V_{OUT} accuracy
- Full-differential current sense across DCR
- AVP - adaptive voltage positioning
- Dual independent adjustable oscillator
- Dual current monitor
- Pre-biased output management
- Average and per-phase OC protection
- OV, UV and FB disconnection protection
- Dual VR_RDY
- WPLGA72 6 x 6 mm package

Applications

- High-current VRM / VRD for desktop / server / workstation Intel® / AMD CPUs
- DDR3 memory supply

Description

The L6751C device is a universal digitally controlled dual PWM DC-DC designed to power Intel's VR12 and AMD SVI processors and memories: all required parameters are programmable through dedicated pin-strapping and PMBus interface. The device features up to 6-phase programmable operation for multi-phase sections and a single-phase with independent control loops. When configured for memory supply, single-phase (VTT) reference is always tracking multi-phase (VDDQ) scaled by a factor of 2. The L6751C supports power state transitions featuring VFDE, programmable DPM and GDC maintaining the best efficiency over all loading conditions without compromising transient response. The device assures fast and independent protection against load overcurrent, under/overvoltage and feedback disconnections.

The device is available in WPLGA72 6 x 6 mm package.

Table 1. Device summary

Order code	Package	Packaging
L6751C	WPLGA72 6 x 6 mm	Tray
L6751CTR	WPLGA72 6 x 6 mm	Tape and reel

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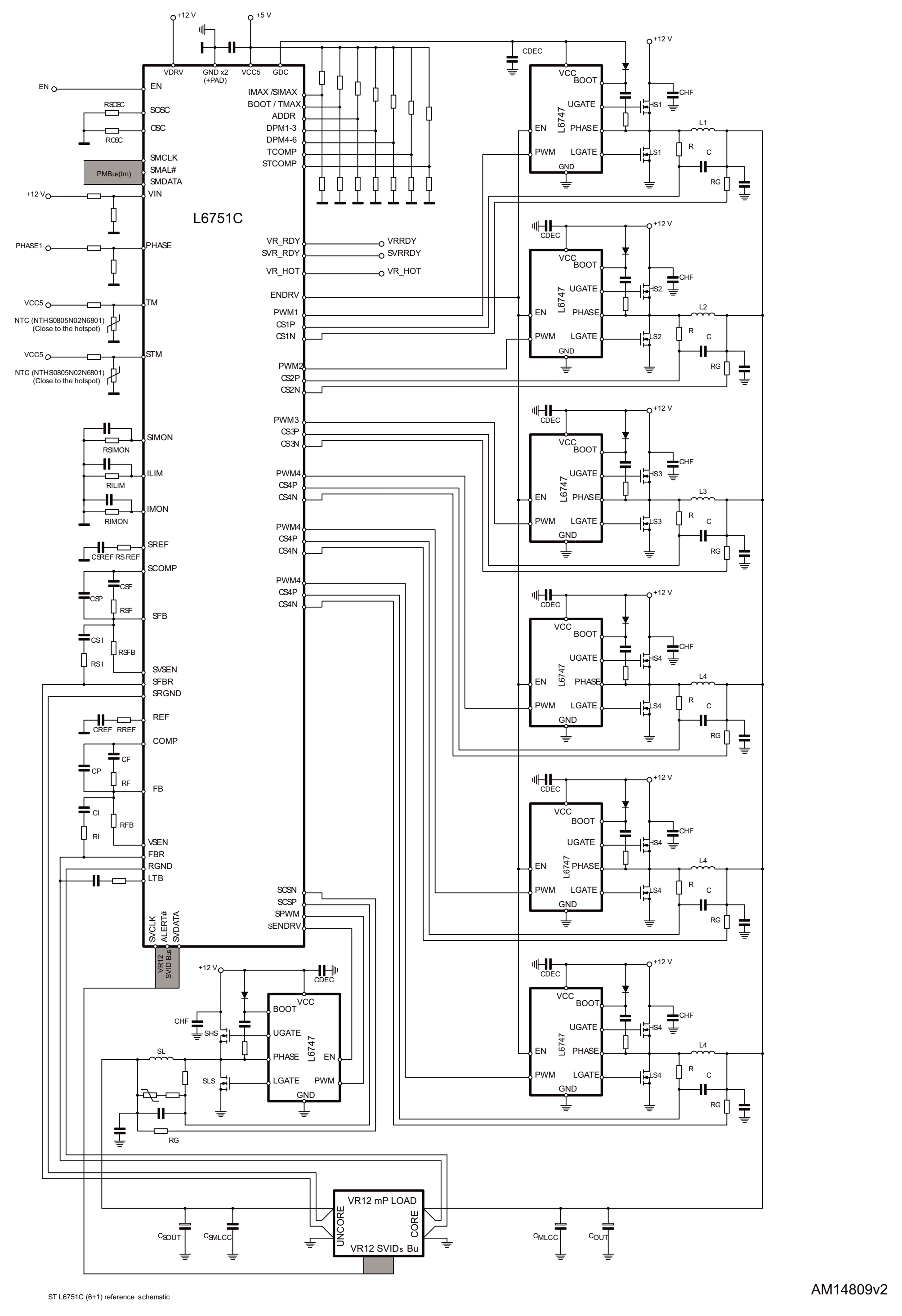
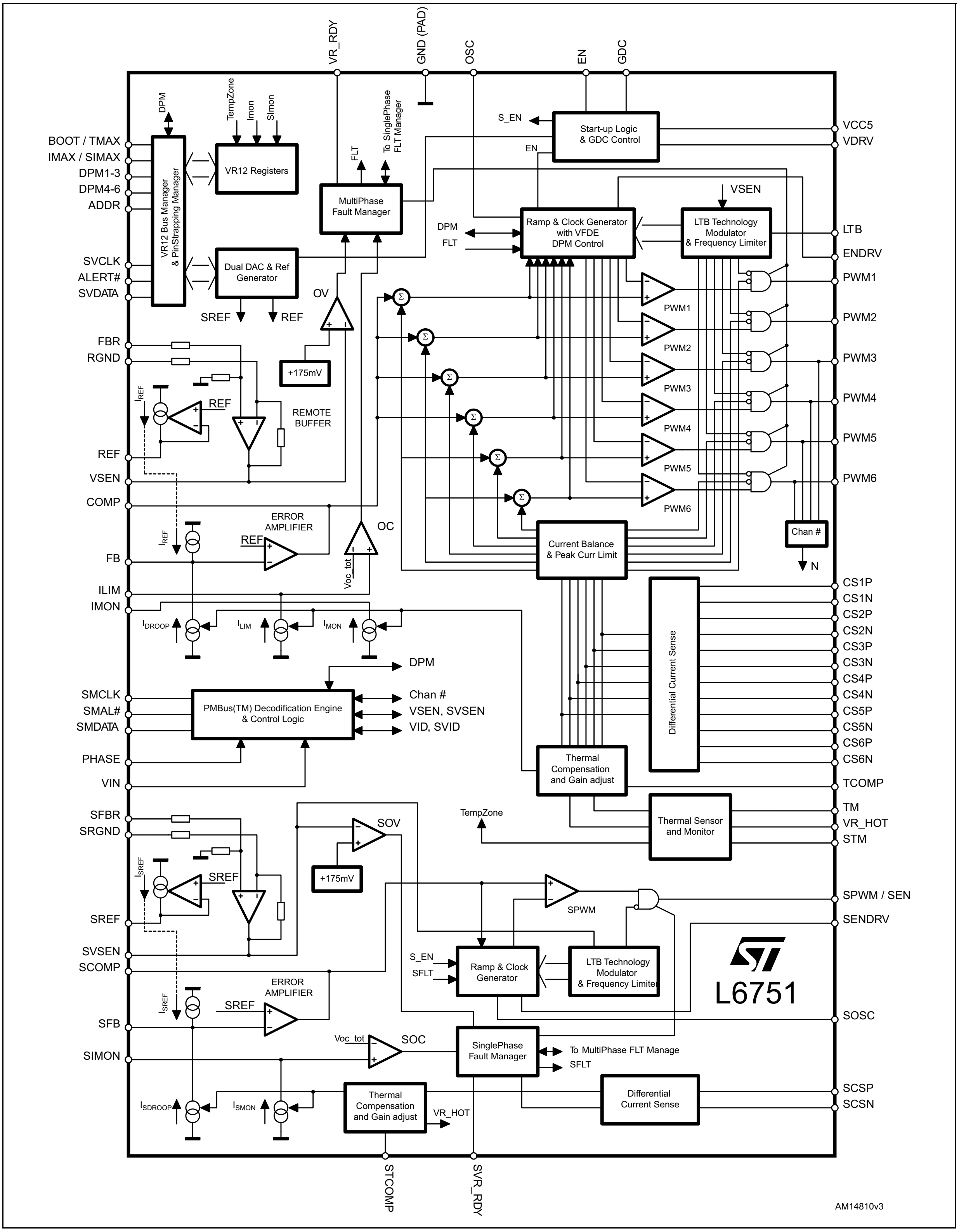
1.1 Application circuit

Figure 1. Typical 6-phase application circuit



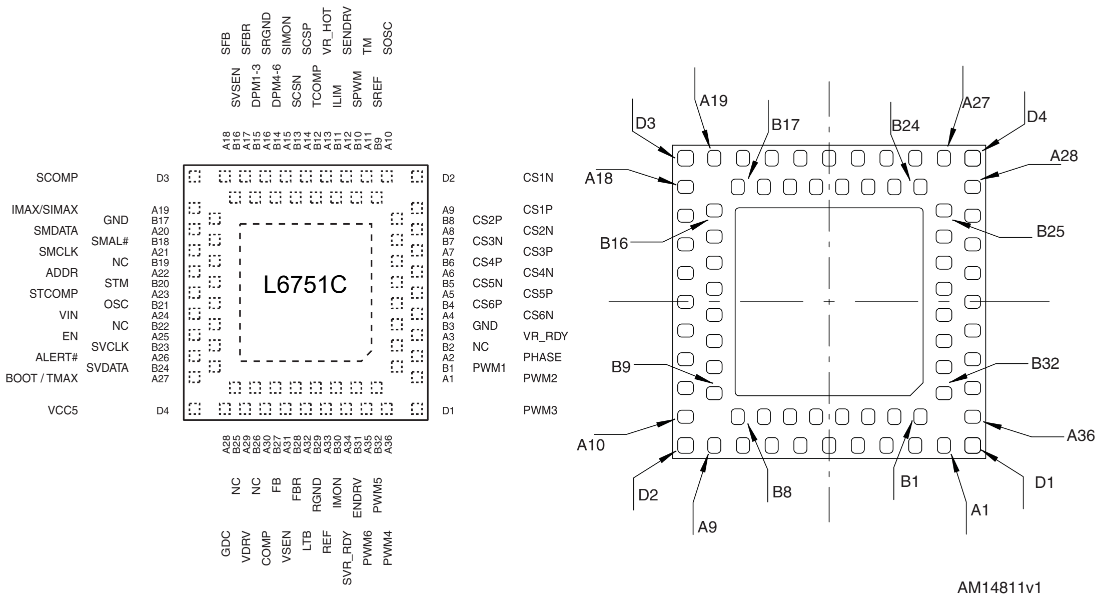
1.2 Block diagram

Figure 2. Block diagram



2 Pin description and connection diagrams

Figure 3. L6751C pin connections (left: top view - right: bottom view)



2.1 Pin description

Table 2. Pin description

Pin no.	Name	Type		Function
D1	PWM3	D(1)	MULTI-PHASE SECTION	PWM output. Connect to multi-phase channel 3 external driver PWM input. During normal operation the device is able to manage Hi-Z status by setting and holding the PWMx pin to a fixed predefined voltage. See *Table 7 on page 20* for phase number programming.
A1	PWM2	D		PWM output. Connect to multi-phase external drivers PWM input. These pins are also used to configure Hi-Z levels for compatibility with drivers and DrMOS. During normal operation the device is able to manage Hi-Z status by setting and holding the PWMx pin to the predefined fixed voltage.
B1	PWM1	D		
A2	PHASE	A		Connect through resistor divider to multi-phase channel1 switching node.
B2	NC	-		Not internally bonded.
A3	VR_RDY	D		VR Ready. Open drain output set free after SS has finished in multi-phase section and pulled low when triggering any protection on multi-phase section. Pull up to a voltage lower than 3.3 V (typ.), if not used it can be left floating.
B3	GND	A		GND connection. All internal references and logic are referenced to this pin. Filter to VCC5 with proper MLCC capacitor and connect to the PCB GND plane.

Table 2. Pin description (continued)

Pin no.	Name	Type		Function
A4	CS6N	A	MULTI-PHASE SECTION	Channel 6 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. When working at < 6 phases, still connect through Rg to CS6P and then to the regulated voltage. Filter the output-side of Rg with 100 nF (typ.) to GND.
B4	CS6P	A		Channel 6 current sense positive input. Connect through an R-C filter to the phase-side of the channel 6 inductor. When working at < 6 phases, short to the regulated voltage.
A5	CS5P	A		Channel 5 current sense positive input. Connect through an R-C filter to the phase-side of the channel 5 inductor. When working at < 5 phases, short to the regulated voltage.
B5	CS5N	A		Channel 5 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. When working at < 5 phases, still connect through Rg to CS5P and then to the regulated voltage. Filter the output-side of Rg with 100 nF (typ.) to GND.
A6	CS4N	A		Channel 4 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. When working at < 4 phases, still connect through Rg to CS4P and then to the regulated voltage. Filter the output-side of Rg with 100 nF (typ.) to GND.
B6	CS4P	A	MULTI-PHASE SECTION	Channel 4 current sense positive input. Connect through an R-C filter to the phase-side of the channel 4 inductor. When working at < 4 phases, short to the regulated voltage.
A7	CS3P	A		Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of the channel 3 inductor. When working at < 3 phases, short to the regulated voltage.
B7	CS3N	A		Channel 3 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. When working at < 3 phases, still connect through Rg to CS3P and then to the regulated voltage. Filter the output-side of Rg with 100 nF (typ.) to GND.
A8	CS2N	A		Channel 2 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND.
B8	CS2P	A		Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of the channel 2 inductor.
A9	CS1P	A		Channel 1 current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor.
D2	CS1N	A		Channel 1 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND.
A10	SOSC	A	SINGLE-PHASE SECTION	Oscillator pin. It allows the switching frequency F_{SSW} to be programmed for the single-phase section. The pin is internally set to 1.02 V, frequency for single-phase is programmed according to the resistor connected to GND or VCC with a gain of 11.5 kHz/µA. Leaving the pin floating programs a switching frequency of 230 kHz. See *Section 10 on page 44* for details.

Table 2. Pin description (continued)

Pin no.	Name	Type		Function
B9	SREF	A	SINGLE-PHASE SECTION	The reference used for the single-phase section regulation is available on this pin with -125 mV offset. Connect through an R_{SREF}-C_{SREF} to GND to optimize DVID transitions. Connect through R_{SOS} resistor to the SFB pin to implement small positive offset to the regulation.
A11	TM	A	MULTI-PHASE SECTION	Thermal monitor sensor. Connect with proper network embedding NTC to the multi-phase power section. The IC senses the power section temperature and uses the information to define the VR_HOT signal and temperature monitoring. By programming proper TCOMP gain, the IC also implements load-line and IMON/ILIM thermal compensation for the multi-phase section. In JMode, the pin disables the single-phase section if shorted to GND. Pull up to VCC5 with 1 kΩ to disable thermal sensor. See *Section 8 on page 39* for details.
B10	SPWM / SEN	D	SINGLE-PHASE SECTION	PWM output. Connect to single-phase external driver PWM input. During normal operation the device is able to manage Hi-Z status by setting and holding the pin to a fixed voltage defined by PWMx strapping. Connect to VCC5 with 1 kΩ to disable the single-phase section.
A12	SENDRV	D	SINGLE-PHASE SECTION	Enable driver. CMOS output driven high when the IC commands the driver. Used in conjunction with the Hi-Z window on the SPWM pin to optimize the single-phase section overall efficiency. Connect directly to external driver enable pin.
B11	ILIM	A	MULTI-PHASE SECTION	Multi-phase section current limit. A current proportional to the multi-phase load current is sourced from this pin. Connect through a resistor R_{LIM} to GND. When the pin voltage reaches 2.5 V, the overcurrent protection is set and the IC latches. Filter through C_{LIM} to GND to delay OC intervention.
A13	VR_HOT	D		Voltage regulator HOT. Open drain output, this is an alarm signal asserted by the controller when the temperature sensed through the ST or TM pins exceed TMAX (active low). See *Section 8 on page 39* for details.
B12	TCOMP	A		Thermal monitor sensor gain. Connect proper resistor divider between VCC5 and GND to define the gain to apply to the signal sensed by the TM to implement thermal compensation for the multi-phase section. Short to GND to disable temperature compensation (but not thermal sensor). See *Section 8 on page 39* for details.

Table 2. Pin description (continued)

Pin no.	Name	Type		Function
A14	SCSP	A	SINGLE-PHASE SECTION	Single-phase section current senses positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor.
B13	SCSN	A		Single-phase section current senses negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND.
A15	SIMON	A		Current monitor output. A current proportional to the single-phase current is sourced from this pin. Connect through a resistor R_{SIMON} to GND. When the pin voltage reaches 1.55 V, overcurrent protection is set and the IC latches. Filtering through C_{SIMON} to GND allows the delay for OC intervention to be controlled.
B14	DPM4-6	A	PINSTRAPPING	Connect a resistor divider to GND/VCC5 in order to define the DPM and GDC strategies. See *Table 11 on page 24* and *Table 12 on page 26* for details.
A16	SRGND	A	SINGLE-PHASE SECTION	Remote buffer ground sense. Connect to the negative side of the single-phase load to perform remote sense.
B15	DPM1-3	A	PINSTRAPPING	Connect a resistor divider to GND/VCC5 in order to define the DPM and GDC strategies. See *Table 11 on page 24* and *Table 12 on page 26* for details.
A17	SFBR	A	SINGLE-PHASE SECTION	Remote buffer positive sense. Connect to the positive side of the single-phase load to perform remote sense.
B16	SVSEN	A		Remote buffer output. Output voltage monitor, manages OV and UV protection. Connect with a resistor R_{SFB} // (R_{SI} - C_{SI}) to SFB.
A18	SFB	A		Error amplifier inverting input. Connect with a resistor R_{SFB} // (R_{SI} - C_{SI}) to SVSEN and with an (R_{SF} - C_{SF})// C_{SH} to SCOMP.
D3	SCOMP	A		Error amplifier output. Connect with an (R_{SF} - C_{SF})// C_{SH} to SFB. The device cannot be disabled by pulling low this pin.
A19	IMAX / SIMAX	A	PINSTRAPPING	Connect a resistor divider to GND/VCC5 in order to define the IMAX and SIMAX registers. See *Table 8 on page 21* and *Table 6 on page 20* for details.

Table 2. Pin description (continued)

Pin no.	Name	Type		Function
B17	GND	A		GND connection. All internal references and logic are referenced to this pin. Filter to VCC5 with proper MLCC capacitor and connect to the PCB GND plane.
A20	SMDATA	D	PMBus	PMBus data.
B18	SMAL#	D		PMBus alert.
A21	SMCLK	D		PMBus clock.
B19	NC	-		Not internally bonded.
A22	ADDR	A	PINSTRAPPING	Connect a resistor divider to GND/VCC5 in order to configure the IC operating mode. See *Table 9 on page 22* and *Table 6 on page 20* for details.
B20	STM	A	SINGLE-PHASE SECTION	Thermal monitor sensor. Connect with proper network embedding NTC to the single-phase power section. The IC senses the power section temperature and uses the information to define the VR_HOT signal and temperature monitoring. By programming proper STCOMP gain, the IC also implements load-line and SIMON thermal compensation for the single-phase section when applicable. Short to GND if not used. See *Section 8 on page 39* for details.
A23	STCOMP	A		Thermal monitor sensor gain. Connect proper resistor divider between VCC5 and GND to define the gain to apply to the signal sensed by ST to implement thermal compensation for the single-phase section. Short to GND to disable temperature compensation. See *Section 8 on page 39* for details.
B21	OSC	A	MULTI-PHASE SECTION	Oscillator pin. It allows the programming of the switching frequency F_{SW} for the multi-phase section. The pin is internally set to 1.02 V, frequency for multi-phase is programmed according to the resistor connected to GND or VCC with a gain of 10 Hz/µA. Leaving the pin floating programs a switching frequency of 200 Hz per phase. Effective frequency observable on the load results as being multiplied by the number of active phases N. See *Section 10 on page 44* for details.
A24	VIN	A		Input voltage monitor. Connect to input voltage monitor point through a divider R_{VUP} / R_{VDWN} to perform VIN sense through PMBus (R_{UP} = 118.5 Ω; R_{DOWN} = 10 kΩ typ.).
B22	NC	-		Not internally bonded.
A25	EN	D		Level sensitive enable pin (3.3 V compatible). Pull low to disable the device, pull up above the turn-on threshold to enable the controller.
B23	SVCLK SVC	D	SVI BUS	Serial clock.
A26	ALERT# V_FIX	D		Alert (Intel mode). V_FIX (AMD mode). Pull to 3.3 V to enter V_FIX mode.

Table 2. Pin description (continued)

Pin no.	Name	Type		Function
B24	SVDATA SVD	D	SVI BUS	Serial data.
A27	BOOT / TMAX	A	PINSTRAPPING	Connect a resistor divider to GND/VCC5 in order to define BOOT and TMAX registers. See *Table 10 on page 23* for details.
D4	VCC5	A		Main IC power supply. Operative voltage is 5 V ± 5%. Filter with 1 µF MLCC to GND (typ.).
A28	GDC	A		Gate drive control pin. Used for efficiency optimization, see *Section 9 on page 41* for details. If not used, it can be left floating. Always filter with 1 µF MLCC to GND.
B25	NC	-		Not internally bonded.
A29	VDRV	A		Driving voltage for external drivers. Connect to the selected voltage rail to drive external MOSFET when in maximum power conditions. IC switches GDC voltage between VDRV and VCC5 to implement efficiency optimization according to selected strategies.
B26	NC	-		Not internally bonded.
A30	COMP / ADDR	A	MULTI-PHASE SECTION	Error amplifier output. Connect with an (R_F - C_F)// C_P to FB. The device cannot be disabled by pulling low this pin. Connect R_{COMP} = 12.5 kΩ to GND to extend PMBus addressing range (see *Table 9 on page 22*).
B27	FB	A		Error amplifier inverting input. Connect with a resistor R_{FB} // (R_I - C_I) to VSEN and with an (R_F - C_F)// C_P to COMP.
A31	VSEN	A		Output voltage monitor, manages OV and UV protection. Connect to the positive side of the load to perform remote sense.
B28	FBR	A		Remote buffer positive sense. Connect to the positive side of the multi-phase load to perform remote sense.
A32	LTB	A		LTB Technology input pin. See *Section 11.2 on page 47* for details.
B29	RGND	A		Remote ground sense. Connect to the negative side of the multi-phase load to perform remote sense.
A33	REF	A		The reference used for the multi-phase section regulation is available on this pin with -125 mV offset. Connect through an R_{REF} - C_{REF} to GND to optimize DVID transitions. Connect through R_{OS} resistor to FB pin to implement small positive offset to the regulation.
B30	IMON	A		Current monitor output. A current proportional to the multi-phase load current is sourced from this pin. Connect through a resistor R_{MON} to GND. The information available on this pin is used for the current reporting and DPM. The pin can be filtered through C_{IMON} to GND.

Table 2. Pin description (continued)

Pin no.	Name	Type		Function
A34	SVR_RDY (PWROK)	D	SINGLE-PHASE SECTION	VR Ready (Intel mode). Open drain output set free after SS has finished and pulled low when triggering any protection for the single-phase section. Pull up to a voltage lower than 3.3 V (typ.), if not used it can be left floating. PowerOK (AMD mode). System-wide Power Good input. When low, the device decodes SVC and SVD to determine the boot voltage.
B31	ENDRV	D	MULTI-PHASE SECTION	Enable driver. CMOS output driven high when the IC commands the drivers. Used in conjunction with the Hi-Z window on the PWMx pins to optimize the multi-phase section overall efficiency. Connect directly to external driver enable pin.
A35	PWM6	D	MULTI-PHASE SECTION	PWM output. Connect to related multi-phase channel external driver PWM input. During normal operation the device is able to manage Hi-Z status by setting and holding the PWMx pin to fixed voltage defined before. See *Table 7 on page 20* for phase number programming.
B32	PWM5	D		
A36	PWM4	D		
PAD	GND	A		GND connection. All internal references and logic are referenced to this pin. Filter to VCC with proper MLCC capacitor and connect to the PCB GND plane.

1. D = digital, A = analog.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal resistance junction-to-ambient (device soldered on 2s2p PC board)	40	°C/W
R_{THJC}	Thermal resistance junction-to-case	1	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	0 to 125	°C

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VDRV, GDC	to GND	-0.3 to 14	V
VCC5, TM, STM, SPWM, PWMx, SENDRV, ENDRV, SCOMP, COMP, SMDATA, SMAL#, SMCLK	to GND	-0.3 to 7	V
All other pins	to GND	-0.3 to 3.6	V

3.2 Electrical characteristics

(V_{CC5} = 5 V ± 5%, T_J = 0 °C to 70 °C unless otherwise specified.)

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{VCC5}	VCC5 supply current	EN = high		28		mA
		EN = low		22		mA
$UVLO_{VCC5}$	VCC5 turn-ON	VCC5 rising			4.1	V
	VCC5 turn-OFF	VCC5 falling	3			V
$UVLO_{VDRV}$	VDRV turn-ON	VDRV rising			6.0	V
	VDRV turn-OFF	VDRV falling	3		4.1	V
$UVLO_{VIN}$	VIN turn-ON	VIN rising, R_{UP} = 118.5 kΩ; R_{DOWN} = 10 kΩ			6.0	V
	VIN turn-OFF	VIN falling, R_{UP} = 118.5 kΩ; R_{DOWN} = 10 kΩ	3		4.1	V
Oscillator, soft-start and enable						
F_{SW}	Main oscillator accuracy	OSC = Open	170	200	230	kHz
	Oscillator adjustability	R_{OSC} / R_{SOSC} = 47 kΩ to GND	378	420	462	kHz
F_{SSW}	Main oscillator accuracy	SOSC = Open	212	250	287	kHz
	Oscillator adjustability	R_{OSC} / R_{SOSC} = 47 kΩ to GND	450	500	550	kHz
ΔV_{OSC}	PWM ramp amplitude(1)			1.5		V
FAULT	Voltage at pin OSC, SSOSC	Latch active for related section	3			V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Soft-start	SS time - Intel CPU mode	Vboot > 0, from pin-strapping; multi-phase section	5			mV/µs
		Vboot > 0, from pin-strapping; single-phase section	2.5			mV/µs
		Vboot > 0, from pin-strapping; single-phase section, JMode ON	2.5			mV/µs
	SS time - Intel DDR mode	Vboot > 0, from pin-strapping; multi-phase section	2.5			mV/µs
		Vboot > 0, from pin-strapping; single-phase section	1.25			mV/µs
	SS time - AMD mode	Vboot > 0, from pin-strapping; both sections		6.25		mV/µs
EN	Turn-ON	V_{EN} rising			0.6	V
	Turn-OFF	V_{EN} falling	0.4			V
	Leakage current			1		µA
SVI serial bus						
SVCLCK, SVDATA	Input high		0.65			V
	Input low				0.45	V
SVDATA, ALERT#	Voltage low (ACK)	I_{SINK} = -5 mA			50	mV
PMBus						
SMDATA, SMCLK	Input high		1.75			V
	Input low				1.45	V
SMAL#	Voltage low	I_{SINK} = -4 mA			13	Ω
Reference and DAC						
k_{VID}	V_{OUT} accuracy (MPhase)	I_{OUT} = 0 A; N = 6; R_G = 540 Ω; R_{FB} = 1.108 kΩ; VID > 1.000 V	-0.5		0.5	%
k_{SVID}	V_{OUT} accuracy (SPhase)	I_{OUT} = 0 A; R_G = 1.3 kΩ; VID > 1.000 V	-0.5		0.5	%
		I_{OUT} = 0 A; R_G = 1.3 kΩ; VID > 1.000 V; JMODE = ON	-5		5	mV
k_{VID}, k_{SVID}	V_{OUT} accuracy	VID = 0.8 V to 1 V	-5		5	mV
		VID < 0.8 V	-8		8	mV
k_{VOUT}	V_{OUT} accuracy - AMD mode		-20		20	mV
Δ_{DROOP}	LL accuracy (MPhase) 0 to full load	I_{INFOx} = 0; N = 6; R_G = 540 Ω; R_{FB} = 1.108 kΩ	-3		2	µA
		The same as above, I_{INFOx} = 20 µA	-4.5		4.5	µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Δ_{SDROOP}	LL accuracy (SPhase) 0 to full load	I_{SCSN} = 0; R_G = 1.3 kΩ	-1.75		1	µA
		I_{SCSN} = 20 µA; R_G = 1.3 kΩ	-1		1	µA
k_{IMON}	IMON accuracy (MPhase)	I_{INFOx} = 0 µA; N = 6; R_G = 540 Ω; R_{FB} = 1.108 kΩ	0		0.75	µA
		Same as above, I_{INFOx} = 20 µA	-4.5		4.5	µA
k_{SIMON}	SIMON accuracy (SPhase)	I_{SCSN} = 0 µA; R_G = 1.3 kΩ	0		0.5	µA
		I_{SCSN} = 20 µA; R_G = 1.3 kΩ	-1		1	µA
A_0	EA DC Gain(1)			100		dB
SR	Slew rate(1)	COMP to SGND = 10 pF		20		V/µs
DVID - Intel CPU mode	Slew rate fast	Multi-phase section	20			mV/µs
	Slew rate slow		5			mV/µs
	Slew rate fast	Single-phase section	10			
	Slew rate slow		2.5			
DVID - Intel DDR mode	Slew rate fast	Multi-phase section	10			mV/µs
	Slew rate slow		2.5			mV/µs
DVID - AMD mode	Slew rate	Both sections		5		mV/µs
IMON ADC	GetReg(15h)	V(IMON) = 0.992 V		CC		Hex
	Accuracy		C0		CF	Hex
PWM outputs and ENDRV						
PWMx, SPWM	Output high	I = 1 mA		5		V
	Output low	I = -1 mA			0.2	V
I_{PWM1}	Test current	Sourced from pin, EN = 0.		10		µA
I_{PWM2}	Test current			0		µA
$I_{PWMx,\ SPWM}$	Test current	Sourced from pin, EN = 0.		-10		µA
ENDRV	Voltage low	I_{ENDRV} = -4 mA; both sections			0.4	V
Protection (both sections)						
OVP	Overvoltage protection	VSEN rising; wrt VID	100		200	mV
UVP	Undervoltage protection	VSEN falling; wrt VID; VID > 500 mV	-525		-375	mV
FBR DISC	FB disconnection	V_{CS-} rising, above VSEN/SVSEN	650	700	750	mV
FBG DISC	FBG disconnection	FBR input wrt VID	950	1000	1050	mV
VR_RDY, SVR_RDY	Voltage low	I_{SINK} = -4 mA			0.4	V
V_{OC_TOT}	OC threshold, MPhase	V_{ILIM} rising, to GND		2.5		V
V_{SOC_TOT}	OC threshold, SPhase	V_{SIMON} rising, to GND		1.55		V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OC_TH}	Constant current[1]	MPhase only		35		µA
VR_HOT	Voltage low	I_{SINK} = -4 mA			13	Ω
Gate drive control						
GDC	Max. current	Any PS.		200		mA
	Impedance	PS00h (GDC = VCC12)		6		Ω
		> PS00h; (GDC = VCC5)		6		Ω

1. Guaranteed by design, not subject to test.

4 Device configuration and pin-strapping tables

The L6751C device features a universal serial data bus fully compliant with Intel VR12/IMVP7 Protocol rev 1.5, document #456098 and AMD SVI specifications, document #40182. To guarantee proper device and CPU operation, refer to these documents for bus design, layout guidelines and any additional information required for the bus architecture. Different platforms may require different pull-up impedance on the SVI bus. Impedance matching and spacing among SVI bus lines must be followed.

The controller configures itself automatically upon detection of different pin-strappings which are monitored at the IC power-up. See *Table 6*, *8*, *9*, *Table 10 on page 23*, and *Table 11 on page 24* for details.

4.1 JMode

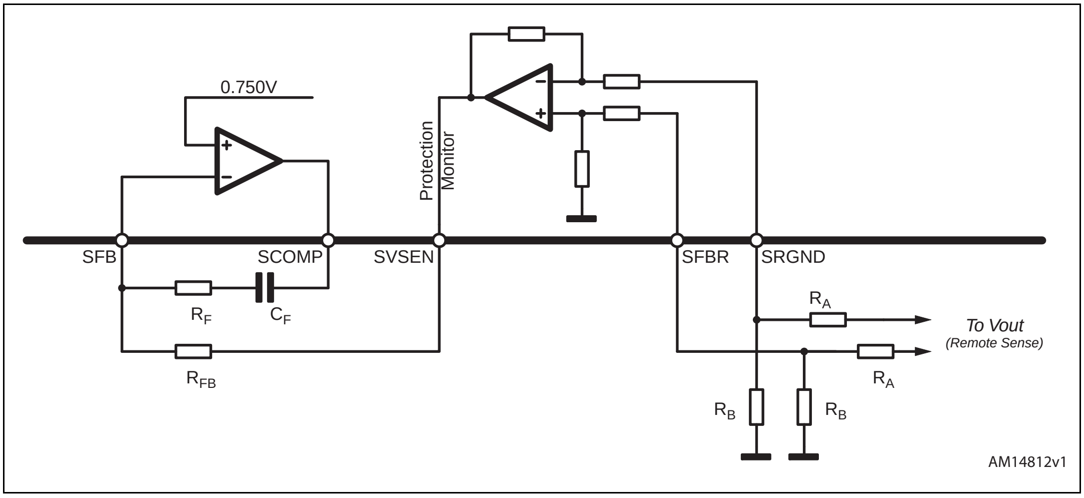
When enabled, multi-phase acts as if in DDR mode, while single-phase is an independent regulator with 0.75 V fixed reference (load-line disabled - TM can be used as enable for the single-phase).

Output voltage higher than the internal reference may be achieved by adding a proper resistor divider (R_A, R_B - see *Figure 4*). To maintain precision in output voltage regulation, it is recommended to provide both SFBR and SRGND with the same divider.

Equation 1

$$V_{OUT} = 0.750 \cdot \frac{R_A + R_B}{R_B}$$

Figure 4. JMode: voltage positioning



4.2 Programming Hi-Z level

The L6751C is able to manage different levels for Hi-Z on PWMx guaranteeing flexibility in driving different external drivers as well as DrMOS ICs.

After EN assertion and before soft-start, the device uses PWM1 and PWM2 to detect the driver/DrMOS connected in order to program the suitable Hi-Z level of PWMx signals. During regulation, the Hi-Z level is used to force the external MOSFETs in high impedance state.

- PWM1 sources a constant 10 µA current, if its voltage results higher than 2.8 V, Hi-Z level used during the regulation is 1.4 V, if lower, PWM2 information is used.
- PWM2 is kept in Hi-Z, if its voltage results higher than 2 V, Hi-Z level used during the regulation is 2 V, if lower, 1.6 V.

An external resistor divider can be placed on PWM1 and PWM2 to force the detection of the correct Hi-Z level. They must be designed considering the external driver/DrMOS selected and the Hi-Z level requested.

Table 6. Device configuration

	SVI address	DROOP (see *Table 8*)	IMAX / SIMAX	BOOT / TMAX	DPM
VR12	0000b	Enabled.	See *Table 8*	See *Table 10*	Supported
VR12(1) ()	0010b 0100b	MPhase: as per *Table 9*. SPhase: disabled			
AMD	n/a	MPhase: enabled. SPhase: as per *Table 9*.	Ignored	TMAX(2) supported	

1. In DDR mode, single-phase reference is multi-phase V_{OUT}/2 (JMode disabled).
2. Refer to *Table 10* and choose any of the resistor combinations leading to the desired TNMAX. Other settings are ignored.

Table 7. Phase number programming

PHASE #	PWM1 to PWM3	PWM4	PWM5	PWM6
3	To driver	1 kΩ to VCC5		
4	To driver		1 kΩ to VCC5	
5	To driver			1 kΩ to VCC5
6	To driver			

Table 8. IMAX, SIMAX pinstrapping(1)

Rdown [kΩ]	Rup [kΩ]	IMAX / SIMAX		
		IMAX [A](2)	SIMAX [A]	
			GFX	VSA/DDR
10	1.5	$N \cdot 25 + 56$	40	29
10	2.7		35	21
22	6.8		30	13
10	3.6		25	5
27	11	$N \cdot 25 + 48$	40	29
12	5.6		35	21
82	43		30	13
13	7.5		25	5
56	36	$N \cdot 25 + 40$	40	29
18	13		35	21
15	12		30	13
18	16		25	5
15	14.7	$N \cdot 25 + 32$	40	29
10	11		35	21
18	22		30	13
56	75		25	5
10	15	$N \cdot 25 + 24$	40	29
12	20		35	21
12	22.6		30	13
39	82		25	5
47	110	$N \cdot 25 + 16$	40	29
10	27		35	21
22	68		30	13
10	36		25	5
18	75	$N \cdot 25 + 8$	40	29
15	75		35	21
10	59		30	13
10	75		25	5
10	100	$N \cdot 25$	40	29
10	150		35	21
10	220		30	13
10	Open		25	5

1. Recommended values, divider needs to be connected between VCC5 pin and GND.
2. N is the number of phase programmed for the multi-phase section.

Table 9. ADDR pin-strapping(1), (2)

Rdown [kΩ]	Rup [kΩ]	ADDR				
		ADDR (3)	PMBADDR(4)	JMode	DROOP multi-phase	DROOP single-phase
10	1.5	AMD mode	CCh	n/a	ON	ON
10	2.7					OFF
22	6.8		C8h			ON
10	3.6					OFF
27	11		C4h			ON
12	5.6					OFF
82	43		C0h			ON
13	7.5					OFF
56	36	0100b (VR12)	EEh	n/a	ON	OFF
18	13				OFF	
15	12		EAh		ON	
18	16				OFF	
15	14.7		E6h		ON	
10	11				OFF	
18	22		E2h		ON	
56	75				OFF	
10	15	0010b (VR12)	ECh	n/a	ON	OFF
12	20				OFF	
12	22.6		E8h		ON	
39	82				OFF	
47	110		E4h		ON	
10	27				OFF	
22	68		E0h		ON	
10	36				OFF	
18	75	0000b (VR12)	CCh / 8Ch	ON	ON	According to VBOOT settings (GFX / VSA)
15	75			OFF		
10	59		C8h / 88h	ON		
10	75			OFF		
10	100		C4h / 84h	ON		
10	150			OFF		

Table 9. ADDR pin-strapping(1), (2) (continued)

Rdown [kΩ]	Rup [kΩ]	ADDR				
		ADDR (3)	PMBADDR(4)	JMode	DROOP multi-phase	DROOP single-phase
10	220	0000b (VR12)	C0h / 80h	ON	ON	According to VBOOT settings (GFX / VSA)
10	Open			OFF		

1. Recommended values, divider needs to be connected between VCC5 pin and GND.
2. In DDR mode, when enabled, droop has 1/4th scaling factor.
3. SVI address for multi-phase. Single-phase is further offset by 0001b. In AMD mode, SVI address defaults according to AMD specifications.
4. PMBus address for multi-phase (read/write). Single-phase is further offset by 02h. When in VR12 CPU mode, RCOMP = 12.5 kΩ to GND, select between Cxh (Open) and 8xh (if installed) PMBus address.

Table 10. BOOT / TMAX pin-strapping(1), (2)

Rdown [kΩ]	Rup [kΩ]	BOOT - Intel address 0000b(3)			Intel address 0010b, 0100b (3)			TMAX [C]
		Multi-phase	Single-phase	Link rest	JMode	VBOOT	Link rest	
10	1.5	1.000 V	0.000 V VSA	32 µsec (debug)	ON	1.500 V	32 µsec (debug)	130
10	2.7							120
22	6.8							110
10	3.6							100
27	11	1.000 V	1.000 V VSA	32 µsec (debug)			10 µsec (functional)	130
12	5.6							120
82	43							110
13	7.5							100
56	36	0.000 V	1.100 V VSA	10 µsec (functional)	ON	1.350 V	32 µsec (debug)	130
18	13							120
15	12							110
18	16							100
15	14.7	0.000 V	1.000 V VSA	10 µsec (functional)			10 µsec (functional)	130
10	11							120
18	22							110
56	75							100

Table 10. BOOT / TMAX pin-strapping(1), (2) (continued)

Rdown [kΩ]	Rup [kΩ]	BOOT - Intel address 0000b(3)			Intel address 0010b, 0100b (3)			TMAX [C]
		Multi-phase	Single-phase	Link rest	JMode	VBOOT	Link rest	
10	15	0.000 V	0.900 V VSA	10 µsec (functional)	OFF	1.500 V	32 µsec (debug)	130
12	20							120
12	22.6							110
39	82							100
47	110	0.000 V	1.000 V GFX	32 µsec (debug)			10 µsec (functional)	130
10	27							120
22	68							110
10	36							100
18	75	1.000 V	1.000 V GFX	32 µsec (debug)	OFF	1.350 V	32 µsec (debug)	130
15	75							120
10	59							110
10	75							100
10	100	0.000 V	0.000 V GFX	10 µsec (functional)			10 µsec (functional)	130
10	150							120
10	220							110
10	Open							100

1. Recommended values, divider needs to be connected between VCC5 pin and GND.
2. BOOT is ignored in AMD mode, only TMAX is operative.
3. Operative mode defined by ADDR pin. See *Table 9* for details.

Table 11. DPM pin-strapping(1)

Rdown [kΩ]	Rup [kΩ]	DPM1-3(2), (3)			DPM4-6(2), (3)		
		DPM12	DPM23	GDC0	DPM34	DPM46	GDC1
10	1.5	16 A	+20 A	1	+30 A	+22 A	1
10	2.7			0			0
22	6.8		+16 A	1		+14 A	1
10	3.6			0			0
27	11		+10 A	1		+8 A	1
12	5.6			0			0
82	43		+6 A	1		DPM OFF	1
13	7.5			0			0

Table 11. DPM pin-strapping(1) (continued)

Rdown [kΩ]	Rup [kΩ]	DPM1-3(2), (3)			DPM4-6(2), (3)		
		DPM12	**DPM23**	**GDC0**	**DPM34**	**DPM46**	**GDC1**
56	36	12 A	+20 A	1	+22 A	+22 A	1
18	13			0			0
15	12		+16 A	1		+14 A	1
18	16			0			0
15	14.7		+10 A	1		+8 A	1
10	11			0			0
18	22		+6 A	1		DPM OFF	1
56	75			0			0
10	15	8 A	+20 A	1	+14 A	+22 A	1
12	20			0			0
12	22.6		+16 A	1		+14 A	1
39	82			0			0
47	110		+10 A	1		+8 A	1
10	27			0			0
22	68		+6 A	1		DPM OFF	1
10	36			0			0
18	75	OFF (12 A)(4)	+20 A	1	+8 A	+22 A	1
15	75			0			0
10	59		+16 A	1		+14 A	1
10	75			0			0
10	100		+10 A	1		+8 A	1
10	150			0			0
10	220		+6 A	1		DPM OFF(5)	1
10	Open			0			0

1. Suggested values, divider needs to be connected between VCC5 pin and GND.
2. Transition threshold specified as delta with respect to previous step (DPM23 is wrt DPM12).
3. GDC threshold is defined by combining GDC0 and GDC1 bits defined between the two different pin-strappings DPM1-3 and DPM4-6. See *Table 12* for details.
4. Transition between 1Phase and 2Phase operation is set to 12 A but disabled in PS00h.
5. Dynamic phase management disabled, IC always working at maximum possible number of phases except from when in >PS00h when transitioning between 1Phase and 2Phase at 12 A.

Table 12. GDC threshold definition(1)

GDC1	GDC0	Threshold [A](2)
1	1	N • 17 A
	0	N • 13 A
0	1	N • 9 A
	0	GDC OFF

1. GDC threshold is defined by combining GDC0 and GDC1 bits defined between the two different pin-strappings DPM1 - 3 and DPM4 - 6. See *Table 11* for details.
2. N is the number of phase programmed for the multi-phase section.

5 Device description and operation

The L6751C device is a programmable 4/5/6-phase PWM controller that provides complete control logic and protection to realize a high performance step-down DC-DC voltage regulator optimized for advanced microprocessor and memory power supply. The device features 2nd generation LTB Technology: through a load transient detector, it is able to turn on simultaneously all the phases. This allows the output voltage deviation to be minimized and, in turn, the system cost to be minimized by providing the fastest response to a load transition.

The L6751C implements current reading across the inductor in fully differential mode. A sense resistor in series to the inductor can also be considered to improve reading precision. The current information read corrects the PWM output in order to equalize the average current carried by each phase.

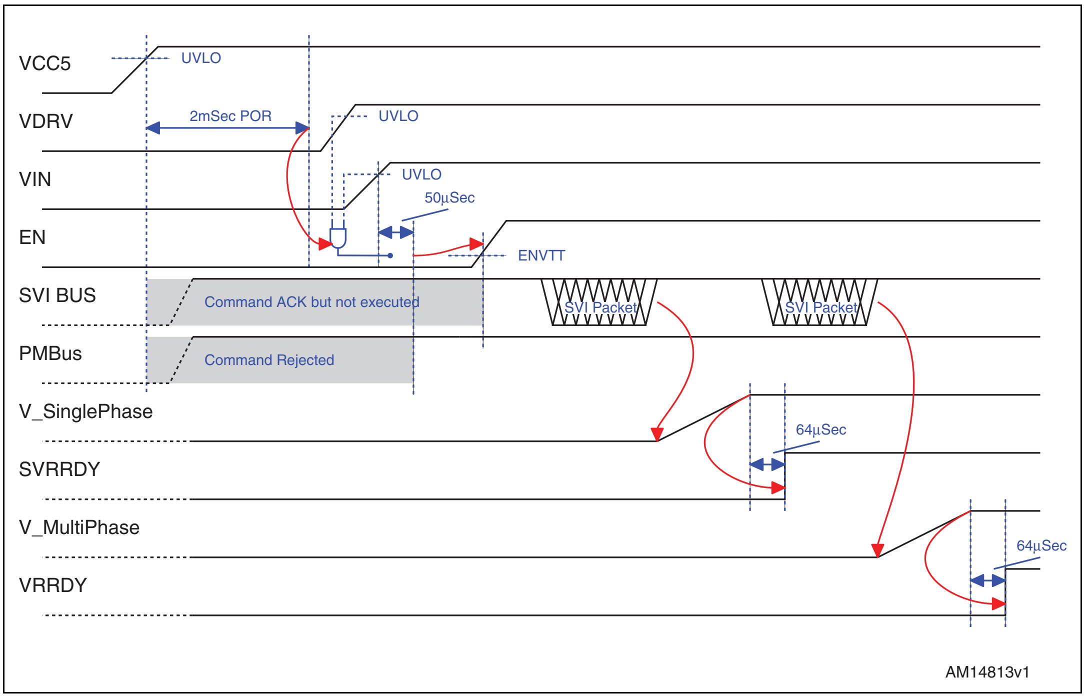
The controller supports Intel and AMD SVI bus and all the required registers. The platform may configure and program the defaults for the device through dedicated pin-strapping.

A complete set of protections is available: overvoltage, undervoltage, overcurrent (per-phase and total), and feedback disconnection guarantees the load to be safe in all circumstances.

Special power management features like DPM, VFDE[a] and GDC modify phase number, gate driving voltage and switching frequency to optimize efficiency over the load range.

The L6751C is available in WPLGA72 6 x 6 mm package.

Figure 5. Device initialization



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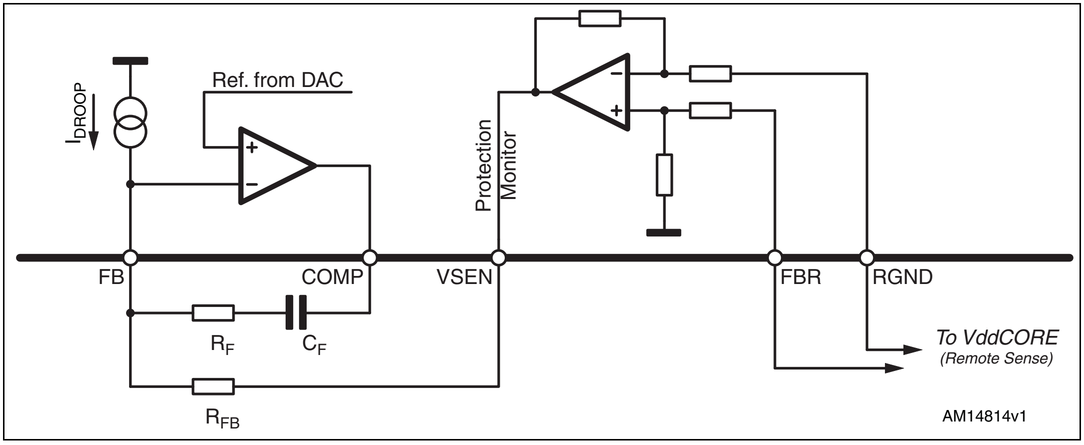
[a] VFDE feature can be enabled using dedicated PMBus command. See *Section 12 on page 48* for details.

6 Output voltage positioning

Output voltage positioning is performed by selecting the controller operative-mode, as per *Table 6 on page 20*, for the two sections and by programming the droop function effect (see *Figure 6*). The controller reads the current delivered by each section by monitoring the voltage drop across the DCR inductors. The current (I_{DROOP} / I_{SDROOP}) sourced from the FB / SFB pins, directly proportional to the read current, causes the related section output voltage to vary according to the external R_{FB} / R_{SFB} resistor, therefore implementing the desired load-line effect.

The L6751C embeds a dual remote-sense buffer to sense remotely the regulated voltage of each section without any additional external components. In this way, the output voltage programmed is regulated compensating for board and socket losses. Keeping the sense traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

Figure 6. Voltage positioning



6.1 Multi-phase section - phase # programming

The multi-phase section implements a flexible 3 to 6 interleaved-phase converter. To proram the desired number of phases, simply short to VCC5 the PWMx signal that is not required, according to *Table 7 on page 20*.

Caution: For the disabled phase(s), the current reading pins need to be properly connected to avoid errors in current-sharing and voltage-positioning: CSxP needs to be connected to the regulated output voltage while CSxN needs to be connected to CSxP through the same R_G resistor used for the active phases.

6.2 Multi-phase section - current reading and current sharing loop

The L6751C embeds a flexible, fully-differential current sense circuitry that is able to read across inductor parasitic resistance or across a sense resistor placed in series to the inductor element. The fully-differential current reading rejects noise and allows the sensing element to be placed in different locations without affecting measurement accuracy. The trans-conductance ratio is issued by the external resistor R_G placed outside the chip between the CSxN pin toward the reading points. The current sense circuit always tracks the current information; the CSxP pin is used as a reference keeping the CSxN pin to this voltage. To correctly reproduce the inductor current, an R-C filtering network must be introduced in parallel to the sensing element. The current that flows from the CSxN pin is then given by the following equation (see *Figure 7*):

Equation 2

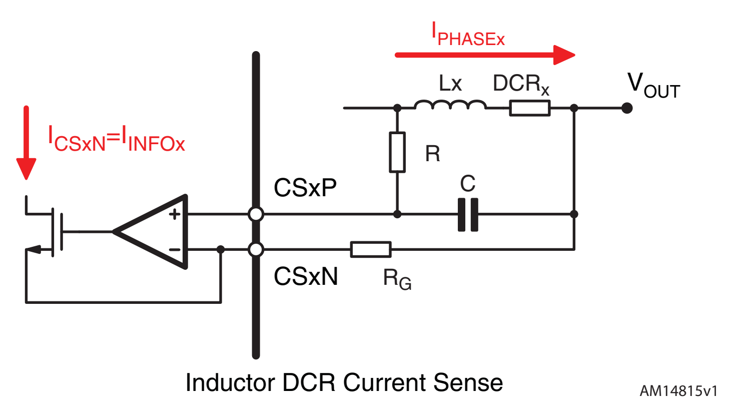
$$I_{CSxN} = \frac{DCR}{R_G} \cdot \frac{1 + s \cdot L / DCR}{1 + s \cdot R \cdot C} \cdot I_{PHASEx}$$

Considering now the matching of the time constant between the inductor and the R-C filter applied (time constant mismatches cause the introduction of poles into the current reading network causing instability. In addition, it is also important for the load transient response and to let the system show resistive equivalent output impedance), it results:

Equation 3

$$\frac{L}{DCR} = R \cdot C \quad \Rightarrow \quad I_{CSxN} = \frac{R_L}{R_G} \cdot I_{PHASEx} = I_{INFOx}$$

Figure 7. Current reading



The current read through the CSxP / CSxN pairs is converted into a current I_{INFOx} proportional to the current delivered by each phase and the information about the average current $I_{AVG} = \Sigma I_{INFOx} / N$ is internally built into the device (N is the number of working phases). The error between the read current I_{INFOx} and the reference I_{AVG} is then converted into a voltage that, with a proper gain, is used to adjust the duty cycle whose dominant value is set by the voltage error amplifier in order to equalize the current carried by each phase.

6.3 Multi-phase section - defining load-line

The L6751C introduces a dependence of the output voltage on the load current recovering part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

Figure 7 shows the current sense circuit used to implement the load-line. The current flowing across the inductor(s) is read through the R-C filter across the CSxP and CSxN pins. R_G programs a trans-conductance gain and generates a current I_{CSx} proportional to the current of the phase. The sum of the I_{CSx} current, with proper gain eventually adjusted by the PMBus commands, is then sourced by the FB pin (I_{DROOP}). R_{FB} gives the final gain to program the desired load-line slope (Figure 6).

Time constant matching between the inductor (L / DCR) and the current reading filter (RC) is required to implement a real equivalent output impedance of the system, therefore avoiding over and/or undershoot of the output voltage as a consequence of a load transient. The output voltage characteristic vs. load current is then given by:

Equation 4

$$V_{OUT} = VID - R_{FB} \cdot I_{DROOP} = VID - R_{FB} \cdot \frac{DCR}{R_G} \cdot I_{OUT} = VID - R_{LL} \cdot I_{OUT}$$

where R_{LL} is the resulting load-line resistance implemented by the multi-phase section.

The R_{FB} resistor can be then designed according to the R_{LL} specifications as follows:

Equation 5

$$R_{FB} = R_{LL} \cdot \frac{R_G}{DCR}$$

Caution: When in DDR mode, and enabled, droop current has a scaling factor equal to 1/4. All the above equations must be scaled accordingly.

6.4 Single-phase section - disable

The single-phase section can be disabled by pulling high the SPWM pin. The related command is rejected.

6.5 Single-phase section - current reading

The single-phase section performs the same differential current reading across DCR as the multi-phase section. According to Section 6.2, the current that flows from the SCSN pin is then given by the following equation (see Figure 7):

Equation 6

$$I_{SCSN} = \frac{DCR}{R_{SG}} \cdot I_{SOUT} = I_{SDROOP}$$

6.6 Single-phase section - defining load-line

This method introduces a dependence of the output voltage on the load current recovering part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

Figure 7 shows the current sense circuit used to implement the load-line. The current flowing across the inductor DCR is read through R_{SG}. R_{SG} programs a trans-conductance gain and generates a current I_{SDROOP} proportional to the current delivered by the single-phase section that is then sourced from the SFB pin with proper gain eventually adjusted by the PMBus commands. R_{SFB} gives the final gain to program the desired load-line slope (*Figure 6*).

The output characteristic vs. load current is then given by:

Equation 7

$$V_{SOUT} = VID - R_{SFB} \cdot I_{SDROOP}$$

$$VID - R_{SFB} \cdot \frac{DCR}{R_{SG}} \cdot I_{SOUT} = VID - R_{SLL} \cdot I_{SOUT}$$

where R_{SLL} is the resulting load-line resistance implemented by the single-phase section.

The R_{SFB} resistor can then be designed according to the R_{SLL} as follows:

Equation 8

$$R_{SFB} = R_{SLL} \cdot \frac{R_{SG}}{DCR}$$

6.7 Dynamic VID transition support

The L6751C manages dynamic VID transitions that allow the output voltage of both sections to be modified during normal device operation for power management purposes. OV, UV and OC signals are masked during every DVID transition and they are re-activated with proper delay to prevent from false triggering.

When changing dynamically the regulated voltage (DVID), the system needs to charge or discharge the output capacitor accordingly. This means that an extra-current I_{DVID} needs to be delivered (especially when increasing the output regulated voltage) and it must be considered when setting the overcurrent threshold of both sections. This current results:

Equation 9

$$I_{DVID} = C_{OUT} \cdot \frac{dV_{OUT}}{dT_{VID}}$$

where dV_{OUT} / dT_{VID} depends on the specific command issued (20 mV/µsec for SetVID_-Fast and 5 mV/µsec for SetVID_Slow). Overcoming the total OC threshold during the dynamic VID causes the device to latch and disable. Set proper filtering on ILIM to prevent from false total-OC tripping.

As soon as the controller receives a new valid command to set the VID level for one (or both) of the two sections, the reference of the involved section steps up or down according to the target-VID with the programmed slope until the new code is reached. If a new valid command is issued during the transition, the device updates the target-VID level and performs the dynamic transition up to the new code. OV, UV are masked during the transition and re-activated with proper delay after the end of the transition to prevent from false triggering.

6.8 LSLESS startup and pre-bias output

Any time the device resumes from an "OFF" code and at the first power-up, in order to avoid any kind of negative undershoot on the load side, the L6751C performs a special sequence in enabling the drivers: during the soft-start phase, the LS driver results as being disabled (LS = OFF - PWMx set to Hi-Z and ENDRV = 0) until the first PWM pulse. After the first PWM pulse, PWMx outputs switch between logic "0" and logic "1" and ENDRV is set to logic "1".

This particular sequence avoids the dangerous negative spike on the output voltage that can occur if starting over a pre-biased output.

Low-side MOSFET turn-on is masked only from the control loop point of view: protection is still allowed to turn on the low-side MOSFET if overvoltage is needed.

Figure 8. LSLESS startup: enabled (left)

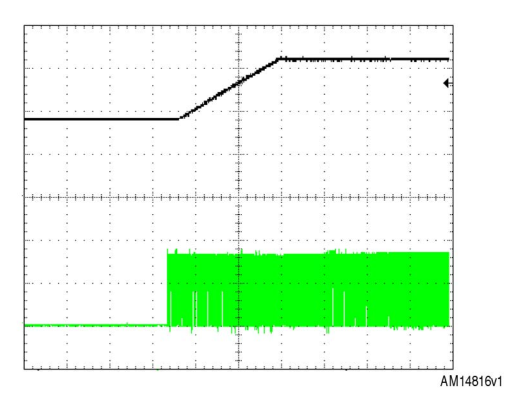
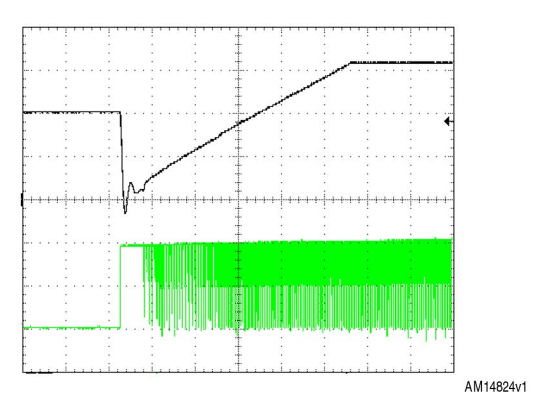


Figure 9. LSLESS startup: disabled (right)



6.9 DVID optimization: REF/SREF

High slew rate for dynamic VID transitions causes undershoot on the regulated voltage, causing violation in the microprocessor requirement. To compensate this behavior and to remove any undershoot in the transition, each section features a DVID optimization circuit.

The reference used for the regulation is available on the REF/SREF pin (see *Figure 10*). Connect an R_{REF}/C_{REF} to GND (R_{SREF}/C_{SREF} for the single-phase) to optimize the DVID behavior. Components may be designed as follows (multi-phase, the same equations apply to single-phase):

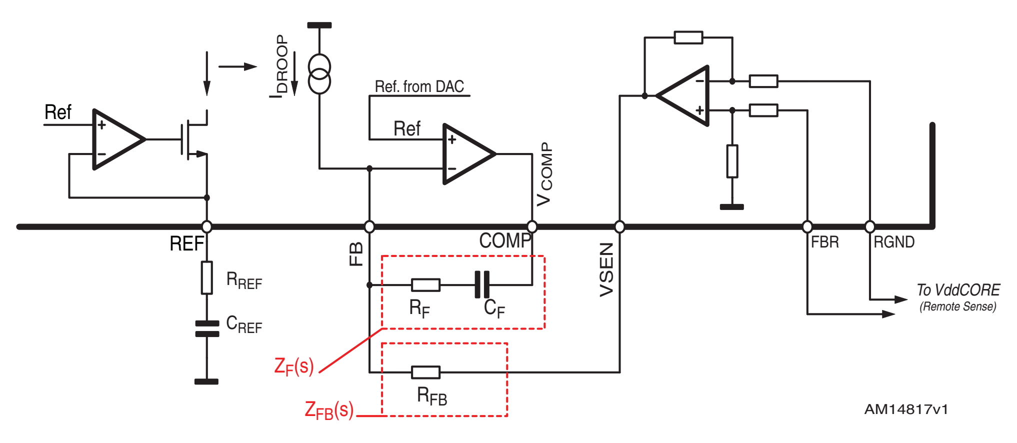
Equation 10

$$C_{REF} = C_F \cdot \left(1 - \frac{\Delta V_{OSC}}{k_V \cdot V_{IN}}\right) \qquad R_{REF} = \frac{R_F \cdot C_F}{C_{REF}}$$

where ΔVosc is the PWM ramp and k_V the gain for the voltage loop (see *Section 11 on page 45*).

During a falling DVID transition, the REF pin moves according to the DVID command issued; the current requested to charge/discharge the R_{REF}/C_{REF} network is mirrored and added to the droop current compensating for undershoot on the regulated voltage.

Figure 10. DVID optimization circuit



7 Output voltage monitoring and protection

The L6751C monitors the regulated voltage of both sections through pin VSEN and SVSEN in order to manage OV and UV. The device shows different thresholds when in different operative conditions but the behavior in response to a protection event is still the same as described below.

Protection is active also during soft-start while it is properly masked during DVID transitions with an additional delay to avoid false triggering. OV protection is active during DVID with threshold modified to 1.8 V unless offset has been commanded by SVI or PMBus: in this case the fixed threshold is 2.4 V.

Table 13. L6751C protection at a glance

	Section	
	Multi-phase	**Single-phase**
Overvoltage (OV)	VSEN, SVSEN = +175 mV above reference. ***Action:*** IC latch; LS = ON and PWMx = 0 (if applicable); other section: Hi-Z. VR_READY of the latched section resets (only).	
Undervoltage (UV)	VSEN, SVSEN = 400 mV below reference. Active after Ref > 500 mV. ***Action:*** IC latch; both sections Hi-Z. VR_READY of the latched section resets (only).	
Overcurrent (OC)	Current monitor across inductor DCR. Dual protection, per-phase and total. ***Action:*** UV-Like. VR_READY of the latched section resets (only).	
Dynamic VID	Protection masked with additional delay to prevent from false triggering.	

7.1 Overvoltage

When the voltage sensed by VSEN and/or SVSEN surpasses the OV threshold, the controller acts in order to protect the load from excessive voltage levels avoiding any possible undershoot. To reach this target, a special sequence is performed as per the following list:

- The reference performs a DVID transition down to 250 mV on the section which triggered the OV protection.
- The PWMs of the section which triggered the protection are switched between Hi-Z and zero (ENDRV is kept high) in order to follow the voltage imposed by the DVID on-going. This limits the output voltage excursion, protects the load and assures no undershoot is generated (if V_{OUT} < 250 mV, the section is Hi-Z).
- The PWMs of the non-involved section are set permanently to Hi-Z (ENDRV is kept low) in order to realize a Hi-Z condition.
- OSC/ FLT pin is driven high.
- Power supply or EN pin cycling is required to restart operation.

If the cause of the failure is removed, the converter ends the transition with all PWMs in Hi-Z state and the output voltage of the section which triggered the protection lower than 250 mV.

7.2 Overcurrent and current monitor

The overcurrent threshold must be programmed to a safe value, in order to be sure that each section does not enter OC during normal operation of the device. This value must take into consideration also the process spread and temperature variations of the sensing elements (inductor DCR).

Furthermore, since also the internal threshold spreads, the design must consider the minimum/maximum values of the threshold.

7.2.1 Multi-phase section

The L6751C features two independent load indicator signals, IMON and ILIM, to properly manage OC protection, current monitoring and DPM. Both IMON and ILIM source a current proportional to the current delivered by the regulator, as follows:

Equation 11

$$I_{MON} = I_{LIM} = \frac{DCR}{R_G} \cdot I_{OUT}$$

The IMON and ILIM pins are connected to GND through a resistor (R_{IMON} and R_{ILIM} respectively), implementing a load indicator with different targets.

- IMON is used for current reporting purposes and for the DPM phase shedding. R_{IMON} must be designed considering that I_{MAX} must correspond to 1.24 V (for correct IMAX detection).
- ILIM is used for the overcurrent protection only. R_{ILIM} must be designed considering that the OC protection is triggered when V(ILIM) = 2.5 V.

In addition, the L6751C also performs per-phase OC protection.

- Per-phase OC. Maximum information current per-phase (I_{INFOx}) is internally limited to 35 μA. This end-of-scale current (I_{OC_TH}) is compared with the information current generated for each phase (I_{INFOx}). If the current information for the single-phase exceeds the end-of-scale current (i.e. if $I_{INFOx} > I_{OC\_TH}$), the device turns on the LS MOSFET until the threshold is re-crossed (i.e. until $I_{INFOx} < I_{OC\_TH}$).
- Total current OC. the ILIM pin allows a maximum total output current for the system (I_{OC_TOT}) to be defined. ILIM current is sourced from the ILIM pin. By connecting a resistor R_{ILIM} to GND, a load indicator with 2.5 V (V_{OC_TOT}) end-of-scale can be implemented. When the voltage present at the ILIM pin crosses V_{OC_TOT}, the device detects an OC and immediately latches with all the MOSFETs of all the sections OFF (Hi-Z).

Typical design considers the intervention of the total current OC before the per-phase OC, leaving this last one as an extreme-protection in case of hardware failures in the external components. Per-phase OC depends on the R_G design while total OC is dependent on the ILIM design and on the application TDC and max. current supported. Typical design flow is the following:

- Define the maximum total output current (I_{OC_TOT}) according to system requirements (I_{MAX}, I_{TDC}). Considering I_{MON} design, I_{MAX} must correspond to 1.24 V (for correct IMAX detection) while considering ILIM design I_{OC_TOT} must correspond to 2.5 V.
- Design per-phase OC and R_G resistor in order to have $I_{INFOx} = I_{OC\_TH}$ (35 μA) when I_{OUT} is about 10% higher than the I_{OC_TOT} current. It results:

Equation 12

$$R_G = \frac{(1.1 \cdot I_{OC\_TOT}) \cdot DCR}{N \cdot I_{OCTH}}$$

where N is the number of phases and DCR the DC resistance of the inductors. R_G should be designed in worst-case conditions.

- Design the R_{IMON} in order to have the IMON pin voltage to 1.24 V at the I_{MAX} current specified by the design. It results:

Equation 13

$$R_{IMON} = \frac{1.24V \cdot R_G}{I_{MAX} \cdot DCR}$$

where I_{MAX} is max. current requested by the processor (see Intel docs for details).

- Design the R_{ILIM} in order to have the ILIM pin voltage to 2.5 V at the I_{OC_TOT} current specified above. It results:

Equation 14

$$R_{ILIM} = \frac{2.5V \cdot R_G}{I_{OC\_TOT} \cdot DCR}$$

where I_{OC_TOT} is the overcurrent switch-over threshold previously defined.

- Adjust the defined values according to application bench testing.
- C_{ILIM} in parallel to R_{ILIM} can be added with proper time constant to prevent false OC tripping and/or delay.
- C_{IMON} in parallel to R_{IMON} can be added to adjust the averaging interval for the current reporting and/or adjust the DPM latencies. Additionally, it can be increased to prevent false total-OC tripping during DVID.

Note: *This is the typical design flow. Custom design and specifications may require different settings and ratios between the per-phase OC threshold and the total current OC threshold. Applications with big ripple across inductors may be required to set per-phase OC to values different than 110%: design flow should be modified accordingly.*

Current reporting precision on IMON may be affected by external layout. The internal ADC is referenced to the device GND pin: in order to perform the highest accuracy in the current monitor, R_{IMON} *must be routed to the GND pin with dedicated net to avoid GND plane drops affecting the precision of the measurement.*

7.2.2 Overcurrent and power states

When the controller receives an SetPS command through the SVI interface, it automatically changes the number of working phases. In particular, the maximum number of phases which L6751C may work in >PS00h is limited to 2 phases regardless of the number N configured in PS00h.

OC level is then scaled as the controller enters >PS00h, as per *Table 14*.

Table 14. Multi-phase section OC scaling and power states

Power state [Hex]	N	OC level (V_{OC_TOT})
00h	3 to 6	2.500 V
01h, 02h	3	1.650 V
	4	1.250 V
	5	1.000 V
	6	0.830 V

7.2.3 Single-phase section

The L6751C performs two different kinds of OC protection for the single-phase section: it monitors both the total current and the per-phase current and allows an OC threshold to be set for both.

- Per-phase OC. Maximum information current per-phase (I_{SINFOx}) is internally limited to 35 μA. This end-of-scale current (I_{SOC_TH}) is compared with the information current generated for each phase (I_{SINFOx}). If the current information for the single-phase exceeds the end-of-scale current (i.e. if $I_{SINFOx} > I_{SOC\_TH}$), the device turns on the LS MOSFET until the threshold is re-crossed (i.e. until $I_{SINFOx} < I_{SOC\_TH}$).
- Total current OC. The SIMON pin allows a maximum total output current for the system (I_{SOC_TOT}) to be defined. I_{SMON} current is sourced from the SIMON pin. By connecting a resistor R_{SIMON} to GND, a load indicator with 1.55 V (V_{SOC_TOT}) end-of-scale can be implemented. When the voltage present at the SIMON pin crosses V_{SOC_TOT}, the device detects an OC and immediately latches with all the MOSFETs of all the sections OFF (Hi-Z).

Typical design considers the intervention of the total current OC before the per-phase OC, leaving this last one as an extreme protection in case of hardware failures in the external components. Total current OC is, moreover, dependent on the SIMON design and on the application TDC and MAX current supported. Typical design flow is the following:

- Define the maximum total output current (I_{SOC_TOT}) according to system requirements (I_{SMAX}, I_{STDC}). Considering I_{SMON} design, I_{SMAX} must correspond to 1.24 V (for correct SIMAX detection) so I_{SOC_TOT} results defined, as a consequence, as $I_{SOC\_TOT} = I_{SMAX} \cdot 1.55 / 1.24$
- Design per-phase OC and R_{SG} resistor in order to have $I_{SINFOx} = I_{SOC\_TH}$ (35 μA) when I_{SOUT} is about 10% higher than the I_{SOC_TOT} current. It results:

Equation 15

$$R_{SG} = \frac{(1.1 \cdot I_{SOC\_TOT}) \cdot DCR}{I_{SOCTH}}$$

where DCR is the DC resistance of the inductors. R_{SG} should be designed in worst-case conditions.

- Design the total current OC and R_{SIMON} in order to have the SIMON pin voltage to 1.24 V at the I_{SMAX} current specified by the design. It results:

Equation 16

$$R_{SIMON} = \frac{1.24V \cdot R_{SG}}{I_{SMAX} \cdot DCR} \qquad \left(I_{SIMON} = \frac{DCR}{R_{SG}} \cdot I_{SOUT}\right)$$

where I_{SMAX} is max. current requested by the processor (see Intel docs for details).

- Adjust the defined values according to application bench tests.
- C_{SIMON} in parallel to R_{SIMON} can be added with proper time constant to prevent false OC tripping.

Note: *This is the typical design flow. Custom design and specifications may require different settings and ratios between the per-phase OC threshold and the total current OC threshold. Applications with big ripple across inductors may be required to set per-phase OC to values different than 110%: design flow should be modified accordingly.*

8 Single NTC thermal monitor and compensation

The L6751C features single NTC for thermal sensing for both thermal monitoring and compensation. Thermal monitor consists in monitoring the converter temperature eventually reporting alarm by asserting the VR_HOT signal. This is the base for the temperature reporting. Thermal compensation consists in compensating the inductor DCR derating with temperature, so preventing drifts in any variable correlated to the DCR: voltage positioning, overcurrent (ILIM), IMON, current reporting. Both the functions share the same thermal sensor (NTC) to optimize the overall application costs without compromising performance. The thermal monitor is featured for both single-phase and multi-phase sections.

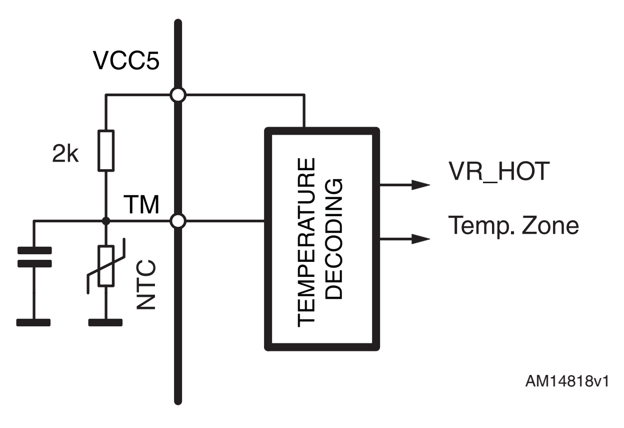
8.1 Thermal monitor and VR_HOT

The diagram for the thermal monitor is reported in *Figure 11*. NTC should be placed close to the power stage hot-spot in order to sense the regulator temperature. As the temperature of the power stage increases, the NTC resistive value decreases, therefore reducing the voltage observable at the TM/STM pin.

Recommended NTC is NTHS0805N02N6801HE for accurate temperature sensing and thermal compensation. Different NTC may be used: to reach the requested accuracy in temperature reporting, the proper resistive network must be used in order to match the resulting characteristic with the one coming from the recommended NTC.

The voltage observed at the TM/STM pin is internally converted and then used for the temperature reporting. When the temperature observed on one of the two thermal sensors exceeds TMAX (programmed via pin-strapping), the L6751C asserts VR_HOT (active low - as long as the overtemperature event lasts).

Figure 11. Thermal monitor connections



8.2 Thermal compensation

The L6751C supports DCR sensing for output voltage positioning: the same current information used for voltage positioning is used to define the overcurrent protection and the current reporting. Having imprecise and temperature-dependent information leads to violation of the specification and misleading information: positive thermal coefficient specific from DCR needs to be compensated to get stable behavior of the converter as temperature increases. Uncompensated systems show temperature dependencies on the regulated voltage, overcurrent protection and current reporting.

The temperature information available on the TM/STM pin and used for thermal monitoring may be used also for this purpose. By comparing the voltage on the TM/STM pin with the voltage present on the TCOMP/STCOMP pin, the L6751C corrects the I_{DROOP}/I_{SDROOP} current used for voltage positioning (see *Section 6.3 on page 29*), so recovering the DCR temperature deviation. Depending on NTC location and distance from the inductors and the available airflow, the correlation between NTC temperature and DCR temperature may be different: TCOMP/STCOMP adjustments allow the gain between the sensed temperature and the correction made on the I_{DROOP}/I_{SDROOP} current to be modified.

Short TCOMP/STCOMP to GND to disable thermal compensation (no correction of I_{DROOP}/I_{SDROOP} is made).

8.3 TM/STM and TCOMP/STCOMP design

This procedure applies to both single-phase and multi-phase sections.

1. Properly choose the resistive network to be connected to the TM pin. Recommended values/network is reported in *Figure 11*.
2. Connect voltage generator to the TCOMP pin (default value 3.3 V).
3. Power on the converter and load the thermal design current (TDC) with the desired cooling conditions. Record the output voltage regulated as soon as the load is applied.
4. Wait for thermal steady-state. Adjust down the voltage generator on the TCOMP pin in order to get the same output voltage recorded at point #3.
5. Design the voltage divider connected to TCOMP (between VCC5 and GND) in order to get the same voltage set to TCOMP at point #4.
6. Repeat the test with the TCOMP divider designed at point #5 and verify the thermal drift is acceptable. In the case of positive drift (i.e. output voltage at thermal steady-state is bigger than output voltage immediately after loading TDC current), change the divider at the TCOMP pin in order to reduce the TCOMP voltage. In the case of negative drift (i.e. output voltage at thermal steady-state is smaller than output voltage immediately after loading TDC current), change the divider at the TCOMP pin in order to increase the TCOMP voltage.
7. The same procedure can be implemented with a variable resistor in place of one of the resistors of the divider. In this case, once the compensated configuration is found, simply replace the variable resistor with a resistor with the same value.

9 Efficiency optimization

As per VR12 specifications, the SVI master may define different power states for the VR controller. This is performed by SetPS commands. The L6751C re-configures itself to improve overall system efficiency, according to *Table 15*.

Table 15. Efficiency optimization

Feature	PS00h	PS01h
DPM	According to pin-strapping	Active. 1Phase/2Phase according to Iout
VFDE	Active when in single-phase and DPM enabled	Active when in single-phase
GDC	12 V driving	GDC set to 5 V

9.1 Dynamic phase management (DPM)

Dynamic phase management allows the number of working phases to be adjusted according to the delivered current still maintaining the benefits of the multi-phase regulation.

Phase number is reduced by monitoring the voltage level across the IMON pin: the L6751C reduces the number of working phases according to the strategy defined by the DPM pin-strapping and/or PMBus (TM) commands received (see *Table 11 on page 24*). DPM12 refers to the current at which the controller changes from 1 to 2 phases. In the same way, DPM23 defines the current at which the controller changes from 2 to 3 phases and so on.

When DPM is enabled, the L6751C starts monitoring the IMON voltage for phase number modification after VR_RDY has transition high: the soft-start is then implemented in interleaving mode with all the available phases enabled.

DPM is reset in the case of an SetVID command that affects the CORE section and when LTB Technology detects a load transient. After being reset, if the voltage across IMON is compatible, DPM is re-enabled after proper delay.

Delay in the intervention of DPM can be adjusted by properly sizing the filter across the IMON pin. Increasing the capacitance results in increased delay in the DPM intervention.

See *Section 7.2.1 on page 35* for guidelines in designing the IMON load indicator.

Note: During load transients with light slope, the filtering of IMON may result too slow for the IC to set the correct number of phases required for the current effectively loading the system (LTB does not trigger in the case of light slopes). The L6751C features a safety mechanism which re-enables phases that were switched off by comparing ILIM and IMON pin voltage. In fact, the ILIM pin is lightly filtered in order to perform fast reaction of OC protection while IMON is heavily filtered to perform correct averaging of the information. While working continuously in DPM, the device compares the information of IMON and ILIM: ILIM voltage is divided in N steps whose width is $V_{OCP}/(2*N)$ *(where* $V_{OCP} = 2.5$ *V and N the number of stuffed phases). If the DPM phase number resulting from IMON is not coherent with the step in which ILIM stays, the phase number is increased accordingly. The mechanism is active only to increase the phase number which is reduced again by DPM.*

9.2 Variable frequency diode emulation (VFDE)

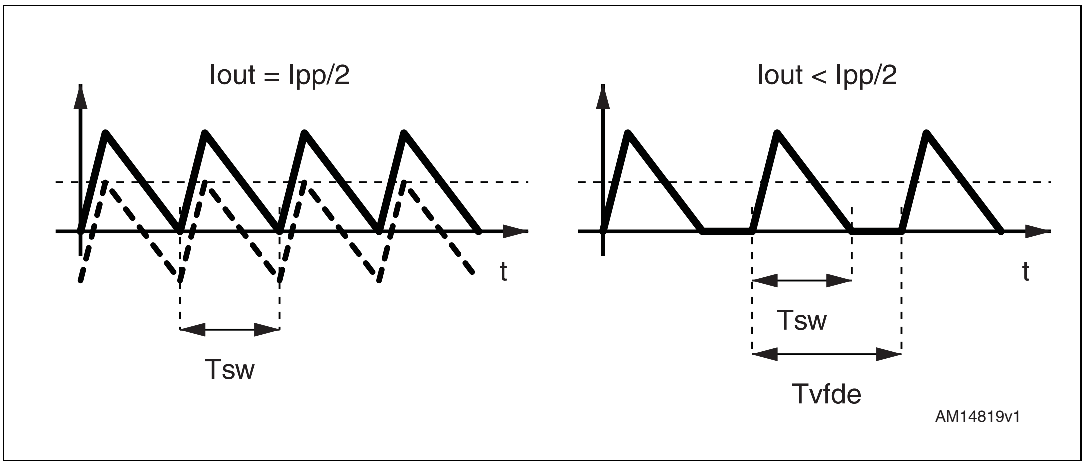
As the current required by the load is reduced, the L6751C progressively reduces the number of switching phases according to DPM settings on the multi-phase section. If single-phase operation is configured, when the delivered current approaches the CCM/DCM boundary, the controller enters VFDE operation. The single-phase section, being a single-phase, enters VFDE operation always when the delivered current approaches the CCM/DCM boundary.

In a common single-phase DC-DC converter, the boundary between CCM and DCM is when the delivered current is perfectly equal to 1/2 of the peak-to-peak ripple into the inductor (Iout = Ipp/2). Further decreasing the load in this condition maintaining CCM operation would cause the current into the inductor to reverse, therefore sinking current from the output for a part of the off-time. This results in a poorly efficient system.

The L6751C device is able (via the CSPx/CSNx pins) to detect the sign of the current across the inductor (zero cross detection, ZCD), so it is able to recognize when the delivered current approaches the CCM/DCM boundary. In VFDE operation, the controller fires the high-side MOSFET for a TON and the low-side MOSFET for a TOFF (the same as when the controller works in CCM mode) and waits the necessary time until next firing in high impedance (Hi-Z). The consequence of this behavior is a linear reduction of the “apparent” switching frequency that, in turn, results in an improvement of the efficiency of the converter when in very light load conditions.

The “apparent” switching frequency reduction is limited to 30 kHz so as not to enter the audible range.

Figure 12. Output current vs. switching frequency in PSK mode



9.3 VFDE and DrMOS

To guarantee correct behavior for the DrMOS power stage compliant with Intel specification rev3, it is recommended to control the DrMOS’ SMOD input through the ENDRV/SENDRV pins of the L6751C. DrMOS enable must be controlled with the same signal used for the L6751C EN pin.

Proper Hi-Z level can be programmed by adding proper external resistor divider across PWM1 and PWM2. See *Section 4.2 on page 20* for details about Hi-Z level recognition. See reference schematic in *Figure 1 on page 6*.

9.4 Gate drive control (GDC)

Gate drive control (GDC) is a proprietary function which allows the L6751C to dynamically control the Power MOSFET driving voltage in order to further optimize the overall system efficiency. According to the SVI power state commanded and the configuration received through the PMBus, the device switches this pin (GDC) between the VCC5 or VDRV (inputs). By connecting the power supply of external drivers directly to this pin, it is then possible to carefully control the external MOSFET driving voltage.

In fact, high driving voltages are required to obtain good efficiency in high loading conditions. On the contrary, in lower loading conditions, such high driving voltage penalizes efficiency because of high losses in Qgs. GDC allows to tune the MOSFET driving voltage according to the delivered current.

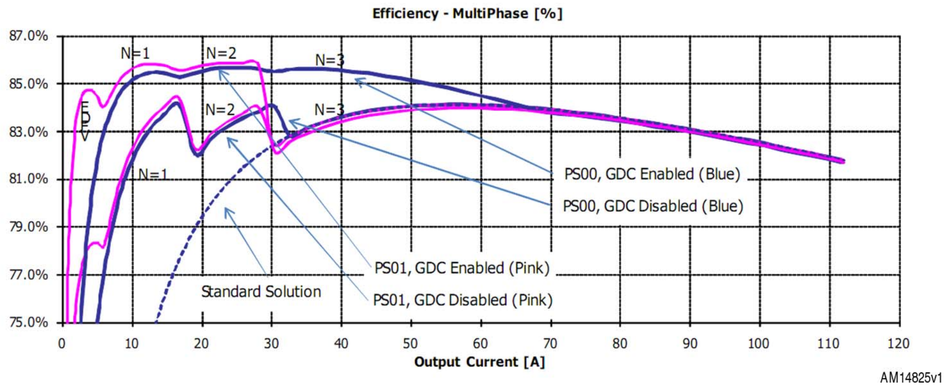
The default configuration considers GDC always switched to VDRV except when entering power states higher than PS01h (included): in this case, to further increase efficiency, simply supply the Phase1 and Phase2 driver through the GDC pin. Their driving voltage is automatically updated as lower power states are commanded through the SVI interface.

Further optimization may be possible by properly setting the automatic GDC threshold through the dedicated PMBus command and/or pin-strapping. It is then possible to enable the gate driving voltage switchover even in PS00h. According to the positioning of the threshold compared with DPM thresholds, it is possible to achieve different performances. Simulations and/or bench tests may be of help in defining the best performing configuration achievable with the active and passive components available.

Figure 13 allows the efficiency improvements with DPM/GDC enabled to be compared with respect to the standard solution.

Note: Systems supporting S3 power state may have the VDRV supplied by an OR-ing connection between 5 Vsby and 12 V or different supply voltage for S0. It is recommended to connect closely, between the VDRV and VCC5 pins, the OR-ing diode connecting VDRV to the 5 Vsby.

Figure 13. Efficiency performance with and without enhancements (DPM, GDC)



10 Main oscillator

The internal oscillator generates the triangular waveform for the PWM charging and discharging, with a constant current, on the internal capacitor. The switching frequency for each channel is internally fixed at 200 kHz (F_{SW}) and at 230 kHz (F_{SSW}): the resulting switching frequency at the load side for the multi-phase section results in being multiplied by N (number of configured phases).

The current delivered to the oscillator is typically 20 µA and may be varied using an external resistor (R_{OSC}, R_{SOSC}) typically connected between the OSC/SOSC pins and GND. Since the OSC/SOSC pins are fixed at 1.02 V, the frequency is varied proportionally to the current sunk from the pin considering the internal gain of 10 KHz/µA for the multi-phase section and of 11.5 kHz/µA for the single-phase section, see *Figure 14*.

Connecting R_{OSC}/R_{SOSC} to SGND, the frequency is increased (current is sunk from the pin), according to the following relationships:

Equation 17

$$F_{SW} = 200\text{kHz} + \frac{1.02\text{V}}{R_{OSC}(\text{k}\Omega)} \cdot 10\frac{\text{kHz}}{\mu\text{A}}$$

Equation 18

$$F_{SSW} = 250\text{kHz} + \frac{1.02\text{V}}{R_{SOSC}(\text{k}\Omega)} \cdot 11.5\frac{\text{kHz}}{\mu\text{A}}$$

Connecting R_{OSC}/R_{SOSC} to a positive voltage Vbias, the frequency is reduced (current is injected into the pin), according to the following relationships:

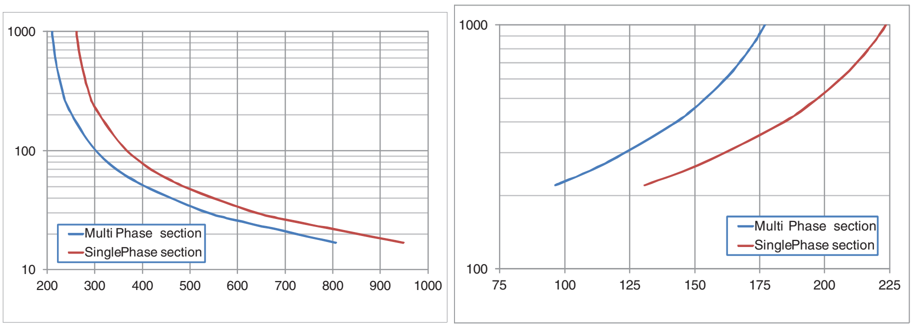
Equation 19

$$F_{SW} = 200\text{kHz} - \frac{\text{Vbias} - 1.02\text{V}}{R_{OSC}(\text{k}\Omega)} \cdot 10\frac{\text{kHz}}{\mu\text{A}}$$

Equation 20

$$F_{SSW} = 250\text{kHz} - \frac{\text{Vbias} - 1.02\text{V}}{R_{SOSC}(\text{k}\Omega)} \cdot 11.5\frac{\text{kHz}}{\mu\text{A}}$$

Figure 14. R_{OSC} vs. F_{SW} per phase (R_{OSC} to GND - left; R_{OSC} to 3.3 V - right)

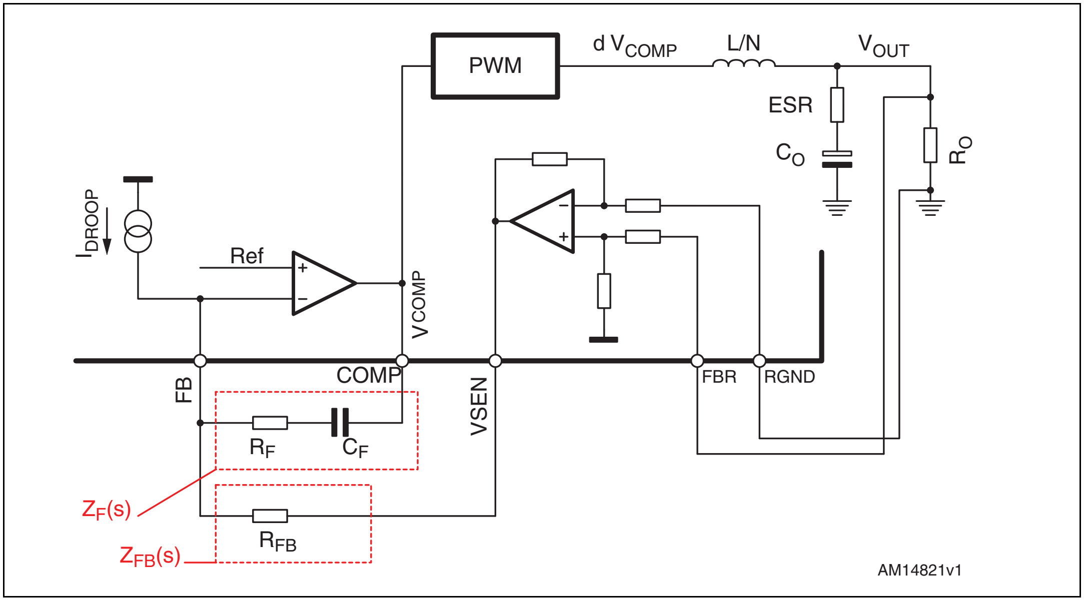


AM14820v1

11 System control loop compensation

The control system can be modeled with an equivalent single-phase converter with the only difference being the equivalent inductor L/N (where each phase has an L inductor and N is the number of the configured phases), see *Figure 15*.

Figure 15. Equivalent control loop



The control loop gain results (obtained opening the loop after the COMP pin):

Equation 21

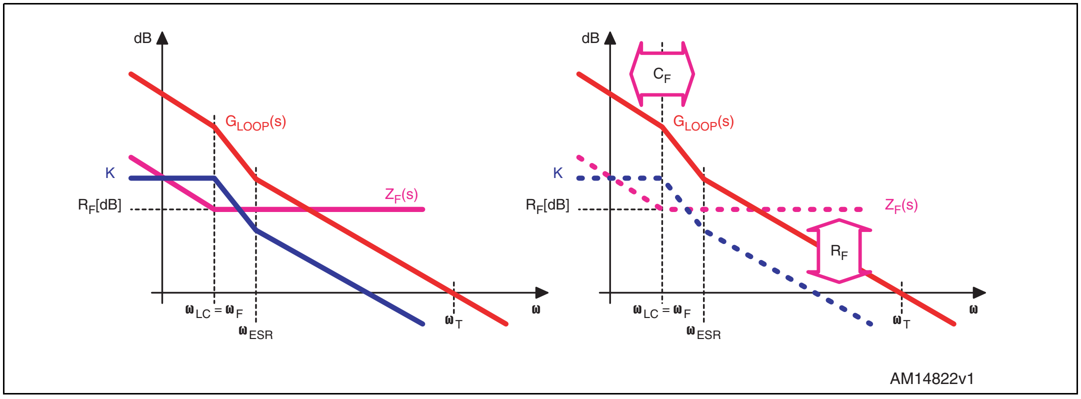
$$G_{LOOP}(s) = -\frac{PWM \cdot Z_F(s) \cdot (R_{LL} + Z_P(s))}{[Z_P(s) + Z_L(s)] \cdot \left[\frac{Z_F(s)}{A(s)} + \left(1 + \frac{1}{A(s)}\right) \cdot R_{FB}\right]}$$

where:

- R_{LL} is the equivalent output resistance determined by the droop function (voltage positioning)
- $Z_P(s)$ is the impedance resulting from the parallel of the output capacitor (and its ESR) and the applied load R_O
- $Z_F(s)$ is the compensation network impedance
- $Z_L(s)$ is the equivalent inductor impedance
- A(s) is the error amplifier gain
- $PWM = \frac{9}{10} \cdot \frac{V_{IN}}{\Delta V_{OSC}}$ is the PWM transfer function.

The control loop gain is designed in order to obtain a high DC gain to minimize static error and to cross the 0 dB axes with a constant -20 dB/dec slope with the desired crossover frequency ω_T. Neglecting the effect of $Z_F(s)$, the transfer function has one zero and two poles; both poles are fixed once the output filter is designed (LC filter resonance ω_{LC}) and the zero (ω_{ESR}) is fixed by ESR and the droop resistance.

Figure 16. Control loop bode diagram and fine tuning



To obtain the desired shape, an R_F - C_F series network is considered for the Z_F(s) implementation. A zero at $\omega_F = 1/R_FC_F$ is then introduced together with an integrator. This integrator minimizes the static error while placing the zero ω_F in correspondence with the L-C resonance and assures a simple -20 dB/dec shape of the gain.

In fact, considering the usual value for the output filter, the LC resonance results as being at a frequency lower than the above reported zero.

The compensation network can be designed as follows:

Equation 22

$$R_F = \frac{R_{FB} \cdot \Delta V_{OSC}}{V_{IN}} \cdot \frac{10}{9} \cdot \frac{F_{SW} \cdot L}{(R_{LL} + ESR)}$$

Equation 23

$$C_F = \frac{\sqrt{C_O \cdot L}}{R_F}$$

11.1 Compensation network guidelines

The compensation network design assures a system response according to the crossover frequency selected and to the output filter considered: it is however possible to further fine tune the compensation network by modifying the bandwidth in order to get the best response of the system as follows (see *Figure 16*):

- Increase R_F to increase the system bandwidth accordingly.
- Decrease R_F to decrease the system bandwidth accordingly.
- Increase C_F to move ω_F to low frequencies, increasing as a consequence the system phase margin.

Having the fastest compensation network does not guarantee that the load requirements are satisfied: the inductor still limits the maximum dI/dt that the system can afford. In fact, when a load transient is applied, the best that the controller can do is to “saturate” the duty cycle to its maximum (d_{MAX}) or minimum (0) value. The output voltage dV/dt is then limited by the inductor charge/discharge time and by the output capacitance. In particular, the most limiting transition corresponds to the load-removal since the inductor results as being discharged only by V_{OUT} (while it is charged by V_{IN} - V_{OUT} during a load appliance).

Note: The introduction of a capacitor (C_I) in parallel to R_{FB} significantly speeds up the transient response by coupling the output voltage dV/dt on the FB pin, so using the error amplifier as a comparator. The COMP pin suddenly reacts and, also thanks to the LTB Technology control scheme, all the phases can be turned on together to immediately give the required energy to the output. Typical design considers starting from values in the range of 100 pF, and validating the effect by bench testing. Additional series resistor (R_I) can also be used.

11.2 LTB Technology

LTB Technology further enhances the performance of the controller by reducing the system latencies and immediately turning on all the phases to provide the correct amount of energy to the load optimizing the output capacitor count.

LTB Technology monitors the output voltage through a dedicated pin detecting load-transients with selected dV/dt, it cancels the interleaved phase-shift, turning on simultaneously all phases.

The LTB detector is able to detect output load transients by coupling the output voltage through an R_{LTB} - C_{LTB} network. After detecting a load transient, all the phases are turned on together and the EA latencies also result as bypassed.

Sensitivity of the load transient detector can be programmed in order to control precisely both the undershoot and the ring-back.

LTB Technology design tips.

- Decrease R_{LTB} to increase the system sensitivity making the system sensitive to smaller dV_{OUT}
- Increase C_{LTB} to increase the system sensitivity making the system sensitive to higher dV/dt
- Increase R_i to increase the width of the LTB pulse
- Increase C_i to increase the LTB sensitivity over frequency.

12 PMBus support (preliminary)

The L6751C device is compatible with PMBus™ standard revision 1.1, refer to PMBus standard documentation for further information (www.pmbus.org).

Table 16. Supported commands

Command	Per rail	Code [Hex]	Mode	Comments
OPERATION	Y	01	RW Byte	Used to turn the controller on/off in conjunction with the input from the control pin. Also used to set margin voltages. Soft off not supported
ON_OFF_CONFIG	N(1)	02	RW Byte	Configures how the controller responds when power is applied
WRITE_PROTECT	Y	10	RW Byte	Controls writing to the PMBus device to prevent accidental changes
VOUT_COMMAND	Y	21	RW Word	Causes the converter to set its output voltage to the commanded value - VID mode
VOUT_MAX	Y	24	RW Word	Sets the upper limit on the output voltage regardless of any other command
VOUT_MARGIN_HIGH	Y	25	RW Word	Sets the voltage to which the output is to be changed when the OPERATION command is set to “margin high”
VOUT_MARGIN_LOW	Y	26	RW Word	Sets the voltage to which the output is to be changed when the OPERATION command is set to “margin low”
IOUT_CAL_OFFSET	Y	39	RW Word	Calibration for IOUT reading
OT_FAULT_LIMIT	Y	4F	RW Word	Overtemperature fault threshold
OT_WARN_LIMIT	Y	51	RW Word	Overtemperature warning threshold
VIN_OV_FAULT_LIMIT	N	55	RW Word	Input voltage monitor overvoltage limit
VIN_UV_FAULT_LIMIT	N	59	RW Word	Input voltage monitor undervoltage limit
MFR_SPECIFIC_01	N	D1	RW Byte	AVERAGE_TIME_SCALE. Sets the time between two measurements
MFR_SPECIFIC_02	Y	D2	RW Byte	DEBUG_MODE. [01/10] Switches [ON/OFF] the V_{OUT} control on PMBus domain
MFR_SPECIFIC_05	Y	D5	RW Byte	VOUT_TRIM. Used to apply a fixed offset voltage to the output voltage command value
MFR_SPECIFIC_08	Y	D8	RW Byte	VOUT_DROOP. Used to change the V_{OUT}droop
MFR_SPECIFIC_35	N(1)	F3	RW Byte	MANUAL_PHASE_SHEDDING. Used to manage the phase shedding manually
MFR_SPECIFIC_38	Y	F6	RW Byte	VOUT_OV_FAULT_LIMIT. Allows the OV protection threshold to be programmed for each rail
MFR_SPECIFIC_39	Y	F7	RW Byte	VFDE_ENABLE
MFR_SPECIFIC_40	Y	F8	RW Byte	ULTRASONIC_ENABLE

Table 16. Supported commands (continued)

Command	Per rail	Code [Hex]	Mode	Comments
MFR_SPECIFIC_41	N(1)	F9	RW Byte	GDC_THRESHOLD. To access the internal register to set GDC threshold [A]
MFR_SPECIFIC_42	N(1)	FA	RW Byte	DPM12_THRESHOLD. To access the internal register to set the DPM12 threshold [A]
MFR_SPECIFIC_43	N(1)	FB	RW Byte	DPM23_THRESHOLD. To access the internal register to set the DPM23 threshold [A]
MFR_SPECIFIC_44	N(1)	FC	RW Byte	DPM34_THRESHOLD. To access the internal register to set the DPM34 threshold [A]
MFR_SPECIFIC_45	N(1)	FD	RW Byte	DPM46_THRESHOLD. To access the internal register to set the DPM46 threshold [A]
CAPABILITY	N	19	R Byte	Provides a way for a host system to determine key capabilities of a PMBus device, such as maximum bus speed and PMBus alert.
VOUT_MODE	N	20	R Byte	The device operates in VID mode
PMBUS_REVISION	N	98	R Byte	Revision of the PMBus which the device is compliant to
MFR_ID	N	99	R Block	Returns the manufacturers ID
MFR_MODEL	N	9A	R Block	Returns manufacturers model number
MFR_REVISION	N	9B	R Block	Returns the device revision number
MFR_SPECIFIC_EXTENDED_COMMAND_00	Y	00	R Byte	VR12_STATUS1
MFR_SPECIFIC_EXTENDED_COMMAND_01	Y	01	R Byte	VR12_STATUS2
MFR_SPECIFIC_EXTENDED_COMMAND_02	Y	02	R Byte	VR12_TEMPZONE
MFR_SPECIFIC_EXTENDED_COMMAND_03	Y	03	R Byte	VR12_IOUT
MFR_SPECIFIC_EXTENDED_COMMAND_05	Y	05	R Byte	VR12_VRTEMP
MFR_SPECIFIC_EXTENDED_COMMAND_07	Y	07	R Byte	VR12_STATUS2_LASTREAD
MFR_SPECIFIC_EXTENDED_COMMAND_08	Y	08	R Byte	VR12_ICCMAX
MFR_SPECIFIC_EXTENDED_COMMAND_09	Y	09	R Byte	VR12_TEMPMAX
MFR_SPECIFIC_EXTENDED_COMMAND_10	Y	0A	R Byte	VR12_SRFAST
MFR_SPECIFIC_EXTENDED_COMMAND_11	Y	0B	R Byte	VR12_SRSLOW
MFR_SPECIFIC_EXTENDED_COMMAND_12	Y	0C	R Byte	VR12_VBOOT

Table 16. Supported commands (continued)

Command	Per rail	Code [Hex]	Mode	Comments
MFR_SPECIFIC_EXTENDED _COMMAND_13	Y	0D	R Byte	VR12_VOUTMAX
MFR_SPECIFIC_EXTENDED _COMMAND_14	Y	0E	R Byte	VR12_VIDSETTING
MFR_SPECIFIC_EXTENDED _COMMAND_15	Y	0F	R Byte	VR12_PWRSTATE
MFR_SPECIFIC_EXTENDED _COMMAND_16	Y	10	R Byte	VR12_OFFSET
CLEAR_FAULTS	N	03	Send Byte	Used to clear any fault bits that have been set
READ_VIN	N	88	R Word	Returns the input voltage in volts (VIN pin)
READ_VOUT	Y	8B	R Word	Returns the actual reference used for the regulation in VID format
READ_IOUT	Y	8C	R Word	Returns the output current in amps
READ_DUTY_CYCLE	N(1)	94	R Word	Returns the duty cycle of the devices main power converter in percentage
MFR_SPECIFIC_04	Y	D4	R Word	READ_VOUT. Returns the actual reference used for the regulation in volts for LINEAR format
READ_TEMPERATURE_1	Y	8D	R Word	READ_TEMPERATURE. [DegC]
STATUS_BYTE	Y	78	R Byte	One byte with information on the most critical faults
STATUS_WORD	Y	79	R Word	Two bytes with information on the units fault condition
STATUS_VOUT	Y	7A	R Byte	Status information on the output voltage warnings and faults
STATUS_IOUT	Y	7B	R Byte	Status information on the output current warnings and faults
STATUS_TEMPERATURE	Y	7D	R Byte	Status information on the temperature warnings and faults
STATUS_CML	Y	7E	R Byte	Status information on the units communication, logic and memory
STATUS_INPUT	N(1)	7C	R Byte	Status information on the input warning and fault
STATUS_MFR_SPECIFIC	Y	80	R Byte	Manufacturer specific status

1. Applies to multi-phase only.

12.1 Enabling the device through PMBus

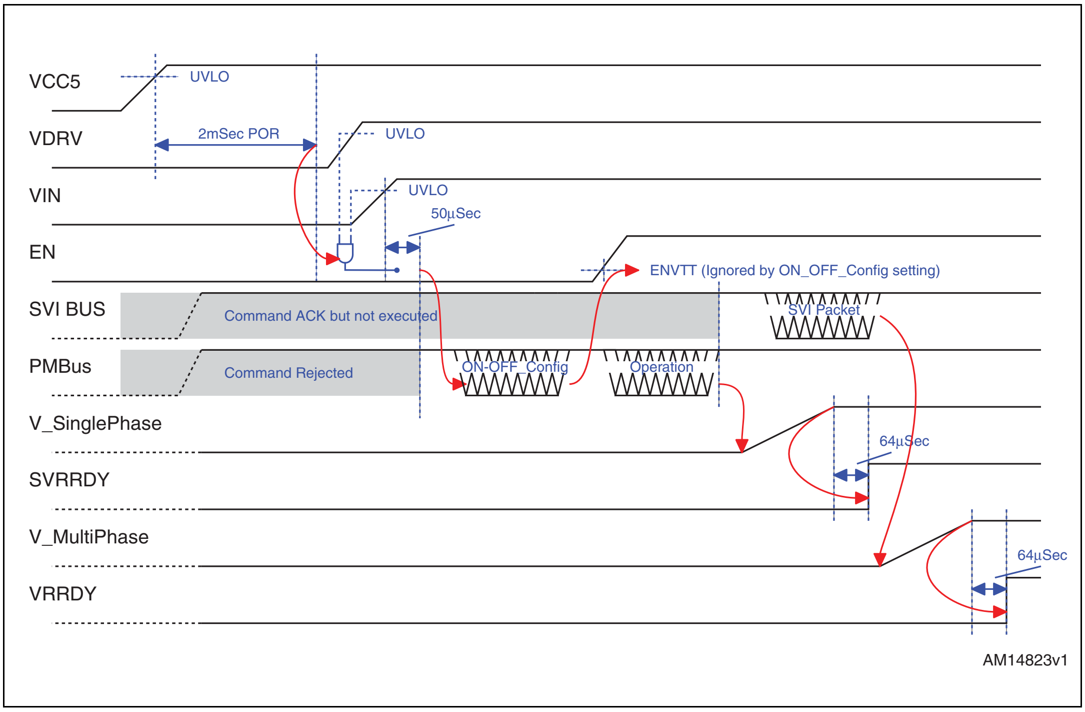
The default condition for the L6751C is to power up through the EN pin ignoring PMBus commands. By properly setting the ON_OFF_CONFIG command, it is also possible to let the device ignore the EN pin acting only as a consequence of the OPERATION command issued.

12.2 Controlling V_{OUT} through PMBus

V_{OUT} can be set independently from SetVID commands issued through the SVI interface by using PMBus. Two main modes can be identified as:

- Offset above SVI commanded voltage. By enabling the MARGIN mode through the OPERATION command and by commanding the MARGIN_HIGH and MARGIN_LOW registers, it is possible to dynamically control an offset above the output voltage commanded through the SVI bus.
- Fixed V_{OUT} regardless of SVI. It is necessary to enter DEBUG_MODE. In this condition, commands from SVI are acknowledged but not executed and VOUT_COMMAND controls the voltage regulated on the output. The L6751C can enter and exit DEBUG_MODE anytime. Upon any transition, V_{OUT} remains unchanged and only the next-coming command affects the output voltage positioning (i.e. when exiting DEBUG_MODE, returning to SVI domain, output voltage remains unchanged until the next SetVID command).

Figure 17. Device initialization: PMBus controlling V_{OUT}



12.3 Input voltage monitoring (READ_VIN)

The dedicated PMBus command allows the user to monitor input voltage. By connecting the VIN pin to the input voltage with the recommended resistor values, the L6751C returns the value of the input voltage measured as a voltage (linear format, N = -4).

The divider needs to be programmed to have 1.24 V on the pin when VIN = 15.9375 V. According to this, R_{UP} = 118.5 kΩ and R_{DOWN} = 10 kΩ.

Errors in defining the divider lead to monitoring errors accordingly.

Filter VIN pin locally to GND to increase stability of the voltage being measured.

12.4 Duty cycle monitoring (READ_DUTY)

The dedicated PMBus command allows the user to monitor duty cycle for multi-phase with the aim of calculating input current inexpensively (no need for input current-sense resistors). By connecting the PHASE pin to the phase1 PHASE pin, the L6751C returns the value of the duty cycle as a percentage (linear format, N = -2).

The divider needs to be programmed to respect absolute maximum ratings for the pin (7 Vmax). According to this, R_{UP} = 5.6 kΩ and R_{DOWN} = 470 Ω.

12.5 Output voltage monitoring (READ_VOUT)

The dedicated PMBus command allows the user to monitor output voltage for both sections. The L6751C returns the value of the programmed VID in VID LSBs (i.e. number of LSBs. C8h = 200 dec x 5 mV = 1.000 V).

12.6 Output current monitoring (READ_IOUT)

The dedicated PMBus command allows the user to monitor output current for both sections. The L6751C returns the value of the delivered current by reading IMON voltage (same as VR12 register 15h) in amperes (linear format, N = 0).

12.7 Temperature monitoring (READ_TEMPERATURE)

The dedicated PMBus command allows the user to monitor the temperature of the power section for multi-phase. The L6751C returns the value of the temperature sensed by NTC connected on the TM/STM pin (the same as VR12 temperature zone) in degrees Celsius (linear format, N = 0).

12.8 Overvoltage threshold setting

The dedicated MFR_SPECIFIC command allows the user to program specific thresholds for multi-phase and single-phase sections.

The threshold can be programmed according to *Table 17*. Different thresholds can be configured for multi-phase and single-phase sections.

Table 17. OV threshold setting

Data byte [Hex]	OC threshold [mV] (above programmed VID)
00h	+175 mV (default)
01h	+225 mV
02h	+275 mV
03h	+325 mV

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13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 18. L6751C WPLGA72 6 x 6 mm package outline

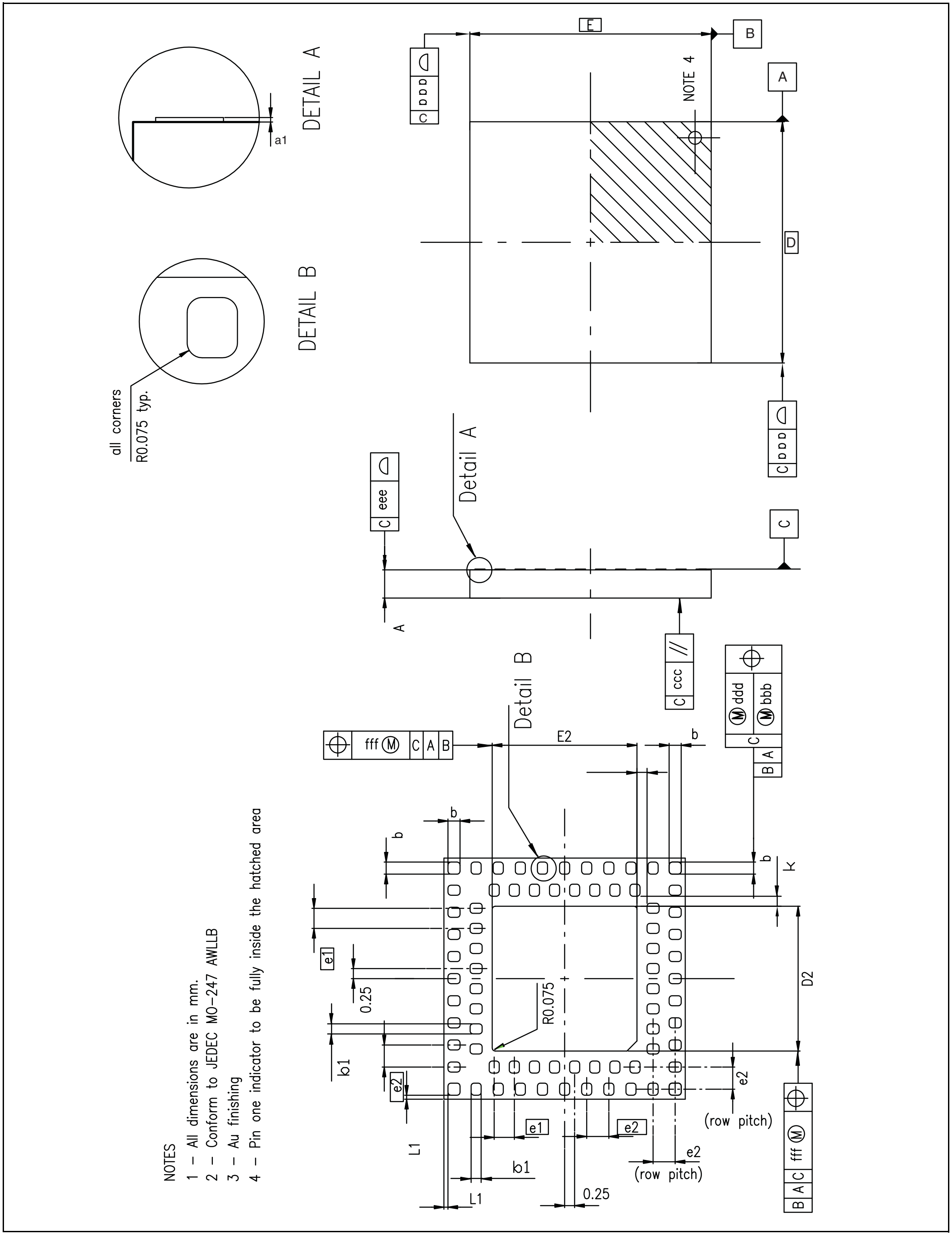

Table 18. L6751C WPLGA72 6 x 6 mm package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.60	0.70	0.80
A1	0.005	0.025	0.045
D		6.00	
D2	3.55	3.60	3.65
E		6.00	
E2	3.55	3.60	3.65
b	0.25	0.30	0.35
b1	0.20	0.25	0.30
e1		0.5	
e2		0.55	
k	0.20	0.25	0.30
L1	0.05		0.15
aaa		0.15	
bbb		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
ccc		0.10	

14 Revision history

Table 19. Document revision history

Date	Revision	Changes
29-Jul-2013	1	Initial release.

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