RENESAS

RMLV0408E Series

4Mb Advanced LPSRAM (512-kword × 8-bit)

R10DS0206EJ0200 Rev.2.00 2016.1.12

Description

The RMLV0408E Series is a family of 4-Mbit static RAMs organized 524,288-word × 8-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV0408E Series has realized higher density, higher performance and low power consumption. The RMLV0408E Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 32-pin SOP, 32-pin TSOP (II) or 32-pin sTSOP.

Features

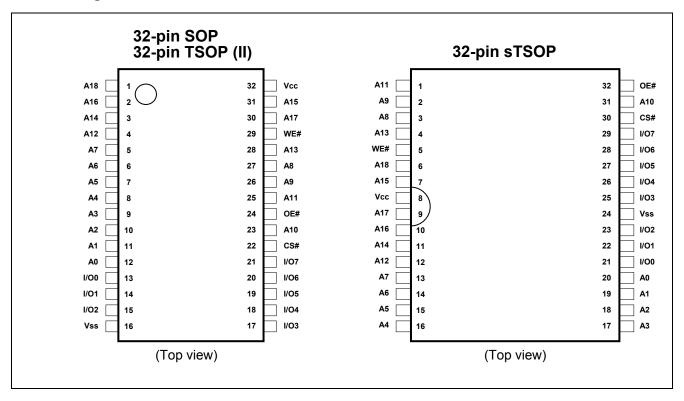
- Single 3V supply: 2.7V to 3.6V
- Access time: 45ns (max.)
- Current consumption: — Standby: 0.4µA (typ.)
- Equal access and cycle times
- Common data input and output — Three state output
- Directly TTL compatible — All inputs and outputs
- Battery backup operation

Orderable part number information

Orderable part number	Access time	Temperature range	Package	Shipping container
RMLV0408EGSA-4S2#AA*			Tray 8mm×13.4mm 32-pin	
RMLV0408EGSA-4S2#KA*			plastic sTSOP	Embossed tape
RMLV0408EGSB-4S2#AA*	45 ns	-40 ~ +85°C	400-mil 32pin	Tray
RMLV0408EGSB-4S2#HA*	45115	-40 % +85 C	plastic TSOP (II)	Embossed tape
RMLV0408EGSP-4S2#CA*			525-mil 32-pin	Tube
RMLV0408EGSP-4S2#HA*			plastic SOP	Embossed tape



Pin Arrangement

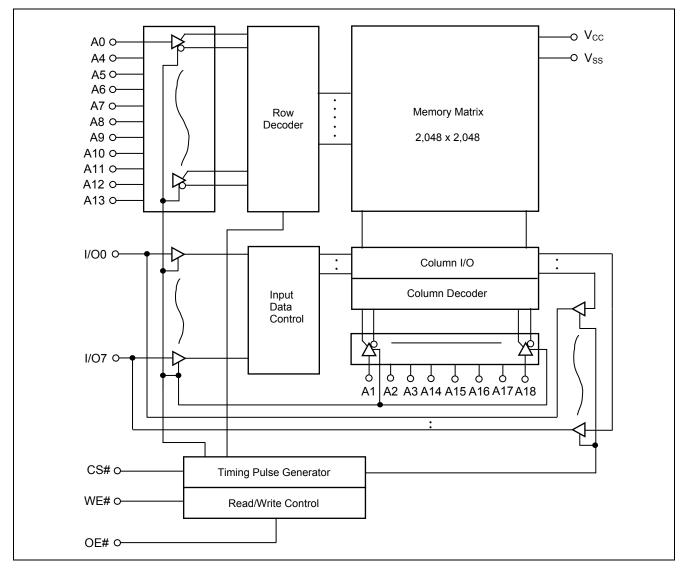


Pin Description

Pin name	Function	
Vcc	Power supply	
V _{SS}	Ground	
A0 to A18	Address input	
I/O0 to I/O7	Data input/output	
CS#	Chip select	
WE#	Write enable	
OE#	Output enable	



Block Diagram



Operation Table

CS#	WE#	OE#	I/O0 to I/O7	Operation
Н	Х	Х	High-Z	Standby
L	Н	L	Dout	Read
L	L	Х	Din	Write
L	Н	Н	High-Z	Output disable

Note 1. H: V_{IH} L:V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V _{SS}	V _{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to $V_{\mbox{\scriptsize SS}}$	VT	-0.5^{*2} to V _{CC} +0.3 ^{*3}	V
Power dissipation	PT	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to +150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note 2. -3.0V for pulse \leq 30ns (full width at half maximum)

3. Maximum voltage is +4.6V.



DC Operating Conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit	Note
Supply voltage	V _{CC}	2.7	3.0	3.6	V	
	V _{SS}	0	0	0	V	
Input high voltage	V _{IH}	2.2	_	V _{CC} +0.3	V	
Input low voltage	VIL	-0.3	_	0.6	V	4
Ambient temperature range	Та	-40	_	+85	°C	

Note 4. -3.0V for pulse \leq 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit		Test conditions		
Input leakage current	I _{LI}	_	-	1	μA	Vin = V _{SS}	to V _{CC}		
Output leakage current	I _{LO}	_	_	1	μΑ	$CS\# = V_{IH} \text{ or } OE\# = V_{IH} \text{ or } WE\# = V_{IL},$ $VI/O = V_{SS} \text{ to } V_{CC}$			
Operating current	I _{CC}	-	Ι	10	mA	CS# =V _{IL} , Others = 1	V _{IH} /V _{IL} , II/O = 0mA		
Average operating current	lasi	_		20	mA	Cycle = 55ns, duty = 100%, II/O = 0m/ CS# = V_{IL} , Others = V_{IH}/V_{IL}			
	I _{CC1}	_	-	25	mA	Cycle = 45ns, duty = 100%, II/O = 0m/ CS# = V_{IL} , Others = V_{IH}/V_{IL}			
	I _{CC2}	_	_	2.5	mA	Cycle = 1µs, duty = 100%, II/O = 0mA CS# \leq 0.2V, V _{IH} \geq Vcc-0.2V, V _{IL} \leq 0.2V			
Standby current	I _{SB}	-	0.1 ^{*5}	0.3	mA	CS# =V _{IH} Others = '	, V _{ss} to V _{CC}		
Standby current		-	0.4 ^{*5}	2	μA	~+25°C			
		-	-	3	μA	~+40°C	Vin = V _{SS} to V _{CC} ,		
	I _{SB1}	-	-	5	μA	~+70°C	$CS# ≥ V_{CC}-0.2V$		
		_	_	7	μA	~+85°C			
Output high voltage	V _{OH}	2.4	_	_	V	I _{он} = -1m.	A		
	V _{OH2}	V _{CC} -0.2	_	_	V	I _{OH} = -0.1	mA		
Output low voltage	V _{OL}	_	_	0.4	V	I _{OL} = 2.1m	۱A		
	V _{OL2}	_	-	0.2	V	I _{OL} = 0.1m	۱A		

Note 5. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25°C), and not 100% tested.

Capacitance

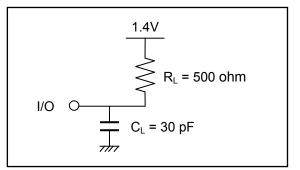
			(Vcc =	2.7V ~ 3	3.6V, f =	= 1MHz, Ta = -4	0 ~ +85°C)
Parameter	Symbol	Min.	Тур.	Max.	Unit	Test conditions	Note
Input capacitance	C in	_	—	8	pF	Vin =0V	6
Input / output capacitance	C 1/0	—	—	10	pF	V _{I/O} =0V	6

Note 6. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc = $2.7V \sim 3.6V$, Ta = $-40 \sim +85^{\circ}C$)

- Input pulse levels: $V_{IL} = 0.4V$, $V_{IH} = 2.4V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	t _{RC}	45	_	ns	
Address access time	t _{AA}	—	45	ns	
Chip select access time	t _{ACS}	—	45	ns	
Output enable to output valid	t _{OE}	—	22	ns	
Output hold from address change	t _{он}	10	—	ns	
Chip select to output in low-Z	t _{CLZ}	10	—	ns	7,8
Output enable to output in low-Z	t _{oLZ}	5	—	ns	7,8
Chip deselect to output in high-Z	t _{CHZ}	0	18	ns	7,8,9
Output disable to output in high-Z	t _{OHZ}	0	18	ns	7,8,9

Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	twc	45	_	ns	
Address valid to write end	t _{AW}	35	_	ns	
Chip select to write end	t _{cw}	35	_	ns	
Write pulse width	t _{WP}	35	_	ns	10
Address setup time to write start	t _{AS}	0	—	ns	
Write recovery time from write end	t _{wr}	0	—	ns	
Data to write time overlap	t _{DW}	25	—	ns	
Data hold from write end	t _{DH}	0	—	ns	
Output enable from write end	tow	5	—	ns	7
Output disable to output in high-Z	t _{онz}	0	18	ns	7,9
Write to output in high-Z	t _{WHZ}	0	18	ns	7,9

Note 7. This parameter is sampled and not 100% tested.

8. At any given temperature and voltage condition, t_{CHZ} max is less than t_{CLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

9. t_{CHZ} , t_{OHZ} and t_{WHZ} are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

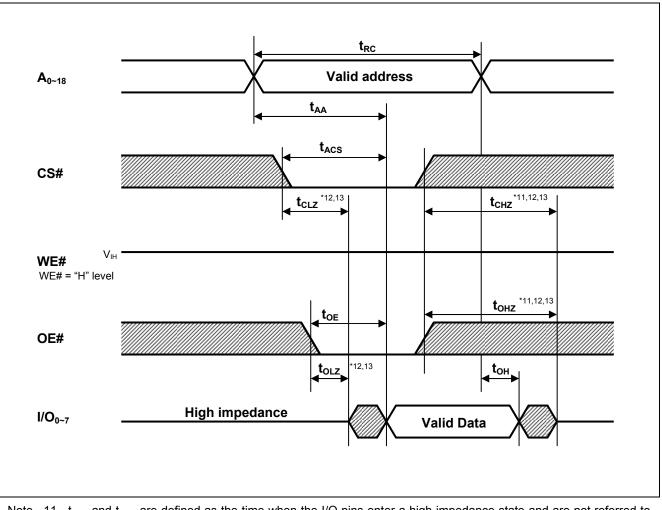
- 10. t_{WP} is the interval between write start and write end.
 - A write starts when both of CS# and WE# become active

A write is performed during the overlap of a low CS#, a low WE#

A write ends when any of CS#, WE# becomes inactive.

Timing Waveforms

Read Cycle

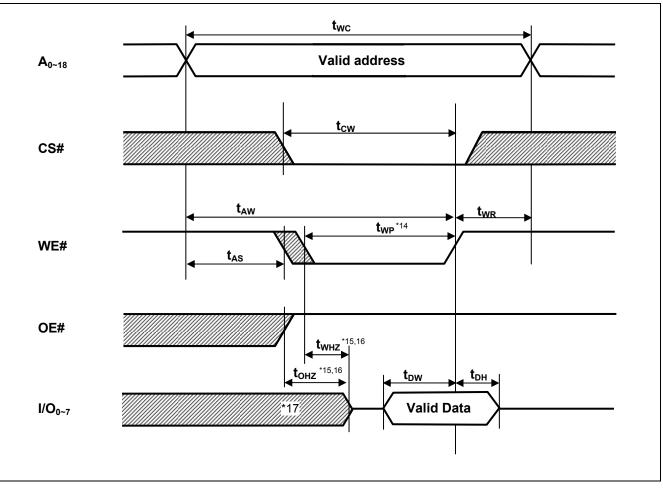


Note 11. t_{CHZ} and t_{OHZ} are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

- 12. This parameter is sampled and not 100% tested.
- 13. At any given temperature and voltage condition, t_{CHZ} max is less than t_{CLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.





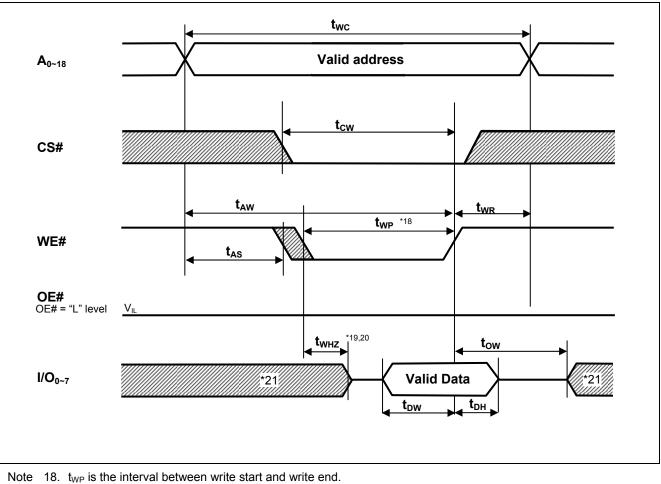


Note 14. t_{WP} is the interval between write start and write end. A write starts when both of CS# and WE# become active. A write is performed during the overlap of a low CS# and a low WE#. A write ends when any of CS# or WE# becomes inactive.

- 15. t_{OHZ} and t_{WHZ} are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.
- 16. This parameter is sampled and not 100% tested.
- 17. During this period, I/O pins are in the output state so input signals must not be applied to the I/O pins.







A write starts when both of CS# and WE# become active.

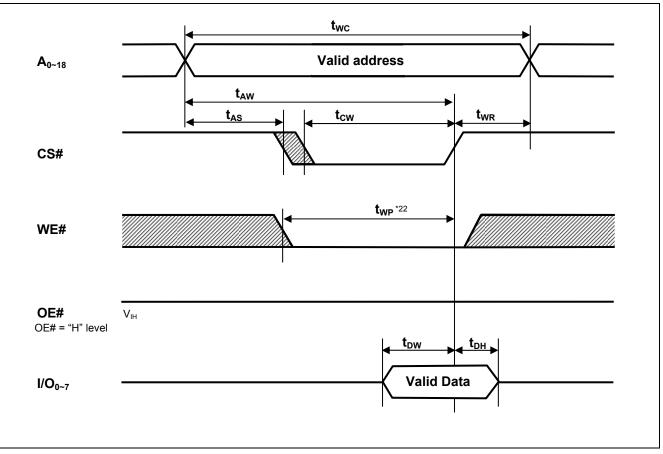
A write is performed during the overlap of a low CS# and a low WE#.

A write ends when any of CS# or WE# becomes inactive.

- 19. t_{WHZ} is defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.
- 20. This parameter is sampled and not 100% tested.
- 21. During this period, I/O pins are in the output state so input signals must not be applied to the I/O pins.



Write Cycle (3) (CS# CLOCK)



Note 22. t_{WP} is the interval between write start and write end.

A write starts when both of CS# and WE# become active.

A write is performed during the overlap of a low CS# and a low WE#.

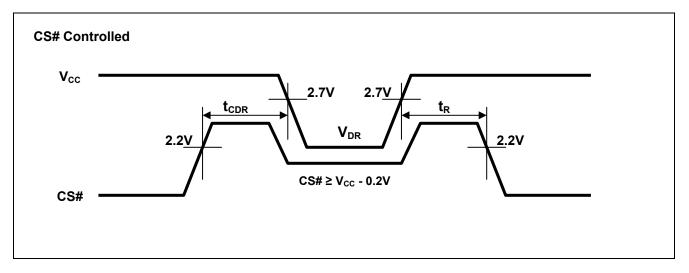
A write ends when any of CS# or WE# becomes inactive.



Parameter	Symbol	Min.	Тур.	Max.	Unit	Test conditions ^{*24}		
V_{CC} for data retention	V_{DR}	1.5	_	_	V	Vin ≥ 0V, CS# ≥ V _{CC} -0.2V		
		_	0.4 ^{*23}	2	μA ~+25°C			
		3 μΑ ~+40°C _{Vcc}		V _{CC} =3.0V, Vin ≥ 0V,				
Data retention current	ICCDR	_	_	5	μA	~+70°C	CS# ≥ Vcc-0.2V	
		_	_	7	μA	~+85°C		
Chip deselect time to data retention	t _{CDR}	0	_	_	ns	Soo roton	tion waveform	
Operation recovery time	t _R	5	_	_	ms	See retention waveform.		

Note 23. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25°C), and not 100% tested.
24. CS# controls address buffer, WE# buffer, OE# buffer, and I/O buffer. If CS# controls data retention mode, Vin levels (address, WE#, OE#, I/O) can be in the high-impedance state.

Low Vcc Data Retention Timing Waveforms (CS# controlled)





Revision History

RMLV0408E Series Data Sheet

		Description	
Rev.	Date	Page	Summary
1.00	2014.2.27	_	First edition issued
2.00	2016.1.12	1	Changed section from "Part Name Information" to "Orderable part number information"

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