MB3771

Power Supply Monitor

Description

The Cypress MB3771 is designed to monitor the voltage level of one or two power supplies (+5 V and an arbitrary voltage) in a microprocessor circuit, memory board in large-size computer, for example.
If the circuit's power supply deviates more than a specified amount, then the MB3771 generates a reset signal to the microprocessor. Thus, the computer data is protected from accidental erasure.
Using the MB3771 requires few external components. To monitor only a +5 V supply, the MB3771 requires the connection of one external capacitor. The level of an arbitrary detection voltage is determined by two external resistors. The MB3771 is available in an 8-pin Dual In-Line, Single In-Line Package or space saving Flat Package.

Features

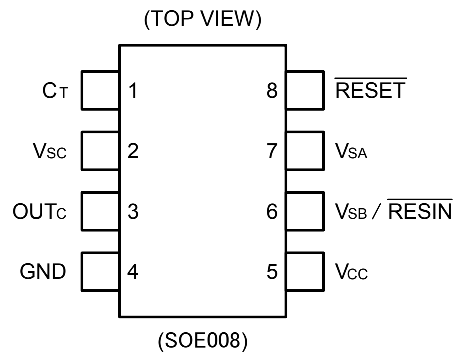
- Precision voltage detection (V_{SA} = 4.2 V ± 2.5 %)
- User selectable threshold level with hysteresis (V_{SB} = 1.23 V ± 1.5 %)
- Monitors the voltage of one or two power supplies (5 V and an arbitrary voltage, >1.23 V)
- Usable as over voltage detector
- Low voltage output for reset signal (V_{CC} = 0.8 V Typ)
- Minimal number of external components (one capacitor Min)
- Low power dissipation (I_{CC} = 0.35 mA Typ, V_{CC} = 5 V)
- Detection threshold voltage has hysteresis function
- Reference voltage is connectable.
- One type of package (SOP-8pin : 1 type)

Application

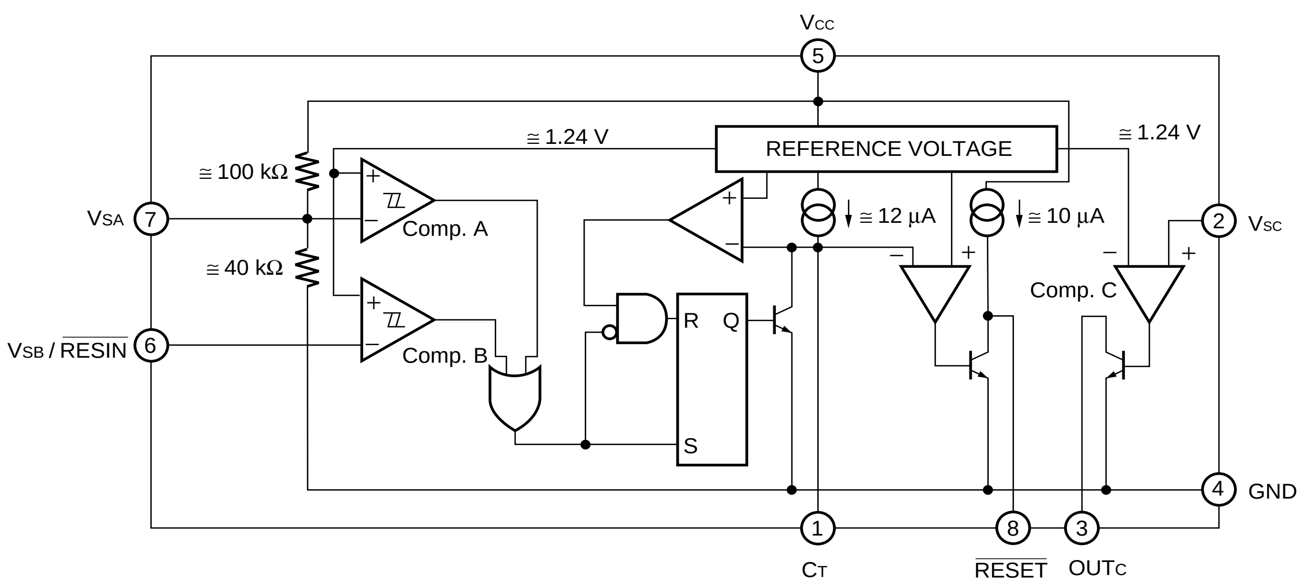
- Industrial Equipment
- Arcade Amusement etc.

Contents

1. Pin Assignment



2. Block Diagram



3. Functional Descriptions

Comparators Comp.A and Comp.B apply a hysteresis to the detected voltage, so that when the voltage at either the V_{SA} or V_{SB} pin falls below 1.23 V the $\overline{\text{RESET}}$ output signal goes to "low" level.

Comp. B may be used to detect any given voltage(8.Application Circuit 8.3 : Arbitrary Voltage Supply Monitor), and can also be used as a forced reset pin (with reset hold time) with TTL input (8.Application Circuit 8.6 : 5V Power Supply Monitor with forced $\overline{\text{RESET}}$ input (V_{CC} = 5 V)).

Note that if Comp.B is not used, the V_{SB} pin should be connected to the V_{CC} pin (8.Application Circuit 8.1 : 5V Power Supply Monitor).

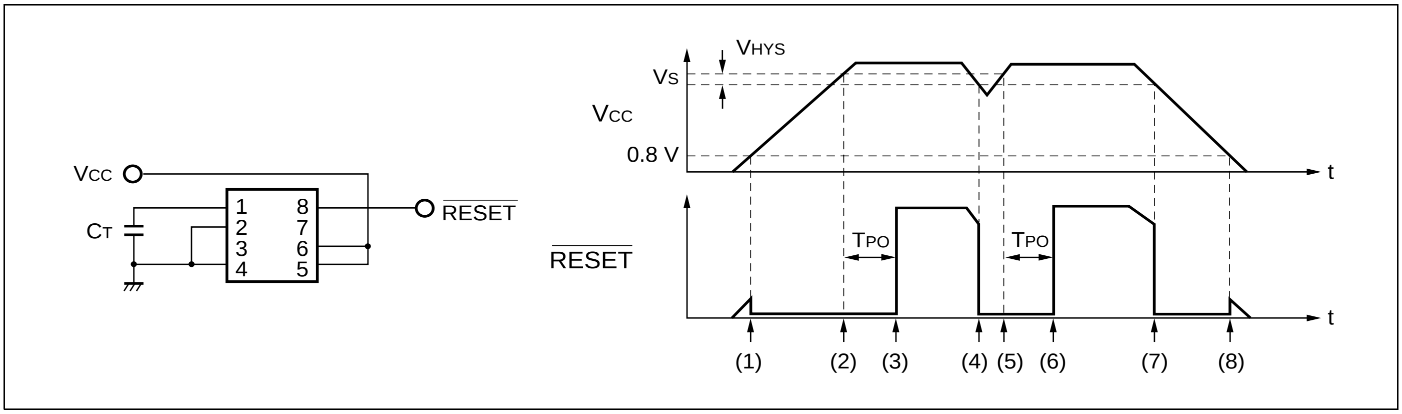
Instantaneous breaks or drops in the power supply can be detected as abnormal conditions by the MB3771 within a 2 µs interval. However because momentary breaks or drops of this duration do not cause problems in actual systems in some cases, a delayed trigger function can be created by connecting capacitors to the V_{SA} or V_{SB} pin (8.Application Circuit 8.8 : Supply Voltage Monitoring with Delayed Trigger).

Because the $\overline{\text{RESET}}$ output has built-in pull-up resistance, there is no need to connect to external pull-up resistance when connected to a high impedance load such as a CMOS logic IC.

Comparator Comp. C is an open-collector output comparator without hysteresis, in which the polarity of input/output characteristics is reversed. Thus Comp. C is useful for over-voltage detection (8.Application Circuit 8.11 : Low Voltage and Over Voltage Detection (V_{CC} = 5 V)) and positive logic $\overline{\text{RESET}}$ signal output (8.Application Circuit 8.7 : 5 V Power Supply Monitor with Non-inverted $\overline{\text{RESET}}$), as well as for creating a reference voltage (8.Application Circuit 8.10 : Reference Voltage Generation and Voltage Sagging Detection).

Note that if Comp. C is not used, the V_{SC} pin should be connected to the GND pin (Application Circuit 1 : 5V Power Supply Monitor).

4. Function Explanation



1. When V_{CC} rises to about 0.8V, $\overline{\text{RESET}}$ goes low.
2. When V_{CC} reaches V_S +V_{HYS}, C_T then begins charging. $\overline{\text{RESET}}$ remains low during this time
3. $\overline{\text{RESET}}$ goes high when CT begins charging.
   $T_{PO} \approx C_T \times 10^5$ (Refer to "C_T pin capacitance vs. reset hold time" in "9.Typical Characteristics".)
4. When V_{CC} level drops lower then V_S, then RESET goes low and C_T starts discharging.
5. When V_{CC} level reaches V_S + V_{HYS}, then C_T starts charging.
   In the case of voltage sagging, if the period from the time V_{CC} goes lower than or equal to V_S to the time V_{CC} reaches V_S +V_{HYS} again, is longer than t_{PI}, (as specified in the 7.2.AC Characteristics), C_T is discharged and charged successively.
6. After T_{PO} passes, and V_{CC} level exceeds V_S + V_{HYS}, then $\overline{\text{RESET}}$ goes high.
7. Same as Point 4.
8. $\overline{\text{RESET}}$ remains low until V_{CC} drops below 0.8V.

5. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage	V_{CC}	−0.3	+20	V
Input voltage	V_{SA}	−0.3	V_{CC} + 0.3 (< +20)	V
	V_{SB}	−0.3	+20	V
	V_{SC}	−0.3	+20	V
Power dissipation	P_D	–	200 (Ta ≤ 85°C)	mW
Storage temperature	Tstg	−55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

6. Recommended Operating Conditions

Parameter	Symbol	Value		Unit
		Min	Max	
Power supply voltage	V_{CC}	3.5	18	V
Output current	$I_{\overline{RESET}}$	0	20	mA
	I_{OUTC}	0	6	mA
Operating ambient temperature	Ta	−40	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.

7. Electrical Characteristics

7.1 DC Characteristics

(V_{CC} = 5 V, Ta = + 25°C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power supply current	I_{CC1}	V_{SB} = 5 V, V_{SC} = 0 V	–	350	500	µA
	I_{CC2}	V_{SB} = 0 V, V_{SC} = 0 V	–	400	600	µA
Detection voltage	V_{SAL} (DOWN)	V_{CC} ↘	4.10	4.20	4.30	V
		Ta = –40°C to +85°C	4.05	4.20	4.35	V
	V_{SAH} (UP)	V_{CC} ↗	4.20	4.30	4.40	V
		Ta = –40°C to +85°C	4.15	4.30	4.45	V
Hysteresis width	V_{HYSA}	–	50	100	150	mV
Detection voltage	V_{SB}	V_{SB} ↘	1.212	1.230	1.248	V
		Ta = –40°C to +85°C	1.200	1.230	1.260	V
Deviation of detection voltage	ΔV_{SB}	V_{CC} = 3.5 V to 18 V	–	3	10	mV
Hysteresis width	V_{HYSB}	–	14	28	42	mV
Input current	I_{IHB}	V_{SB} = 5 V	–	0	250	nA
	I_{ILB}	V_{SB} = 0 V	–	20	250	nA
Output voltage	V_{OHR}	$I_{\overline{RESET}}$ = –5 µA, V_{SB} = 5 V	4.5	4.9	–	V
	V_{OLR}	$I_{\overline{RESET}}$ = 3mA, V_{SB} = 0 V	–	0.28	0.4	V
		$I_{\overline{RESET}}$ = 10mA, V_{SB} = 0 V	–	0.38	0.5	V
Output sink current	$I_{\overline{RESET}}$	V_{OLR} = 1.0 V, V_{SB} = 0 V	20	40	–	mA
CT charge current	I_{CT}	V_{SB} = 5 V, V_{CT} = 0.5 V	9	12	16	µA
Input current	I_{IHC}	V_{SC} = 5 V	–	0	500	nA
	I_{ILC}	V_{SC} = 0 V	–	50	500	nA
Detection voltage	V_{SC}	–	1.225	1.245	1.265	V
		Ta = –40°C to +85°C	1.205	1.245	1.285	V
Deviation of detection voltage	ΔV_{SC}	V_{CC} = 3.5 V to 18 V	–	3	10	mV
Output leakage current	I_{OHC}	V_{OHC} = 18 V	–	0	1	µA
Output voltage	V_{OLC}	I_{OUTC} = 4 mA, V_{SC} = 5 V	–	0.15	0.4	V
Output sink current	I_{OUTC}	V_{OLC} = 1.0 V, V_{SC} = 5 V	6	15	–	mA
Reset operation minimum supply voltage	V_{CCL}	V_{OLR} = 0.4 V, $I_{\overline{RESET}}$ = 200 µA	–	0.8	1.2	V

7.2 AC Characteristics

(V_{CC} = 5 V, Ta = + 25°C, C_T = 0.01 μF)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
V_{SA}, V_{SB} input pulse width	t_{PI}	–	5.0	–	–	μs
Reset hold time	t_{PO}	–	0.5	1.0	1.5	ms
$\overline{RESET}$ rise time	t_r	R_L = 2.2 kΩ, C_L = 100 pF	–	1.0	1.5	μs
$\overline{RESET}$ fall time	t_f		–	0.1	0.5	μs
Propagation delay time	t_{PD}*1	–	–	2	10	μs
	t_{PHL}*2	R_L = 2.2 kΩ, C_L = 100 pF	–	0.5	–	μs
	t_{PLH}*2		–	1.0	–	μs

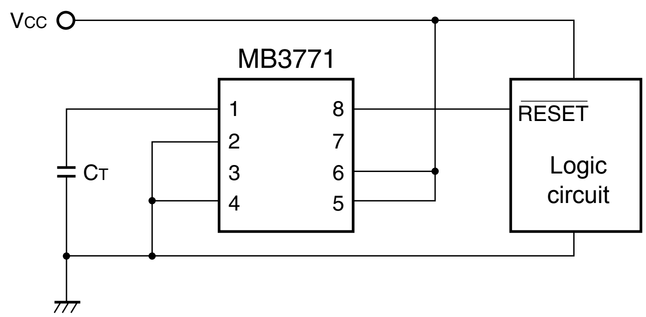
*1: In case of V_{SB} termination.

*2: In case of V_{SC} termination.

8. Application Circuit

8.1 5V Power Supply Monitor

Monitored by V_{SA}. Detection threshold voltage is V_{SAL} and V_{SAH}



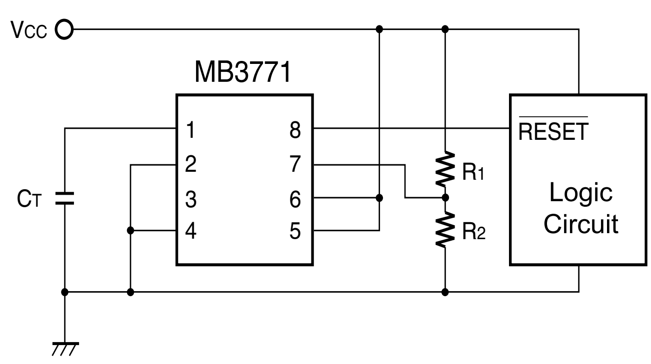
8.2 5V Power Supply Voltage Monitor (Externally Fine-Tuned Type)

The V_{SA} detection voltage can be adjusted externally.

Resistance R_1 and R_2 are set sufficiently lower than the IC internal partial voltage resistance, so that the detection voltage can be set using the ratio between resistance R_1 and R_2. (Refer to the table below).

- R_1, R_2 calculation formula (when R_1 << 100 kΩ, R_2 <<40 kΩ)
  $V_{SAL} \approx (R_1 + R_2) \times V_{SB} / R_2$ [V], $V_{SAH} \approx (R_1 + R_2) \times (V_{SB} + V_{HYSB}) / R_2$ [V]

R_1 (kΩ)	R_2 (kΩ)	Detection voltage : V_{SAL} (V)	Detection voltage : V_{SAH} (V)
10	3.9	4.37	4.47
9.1	3.9	4.11	4.20

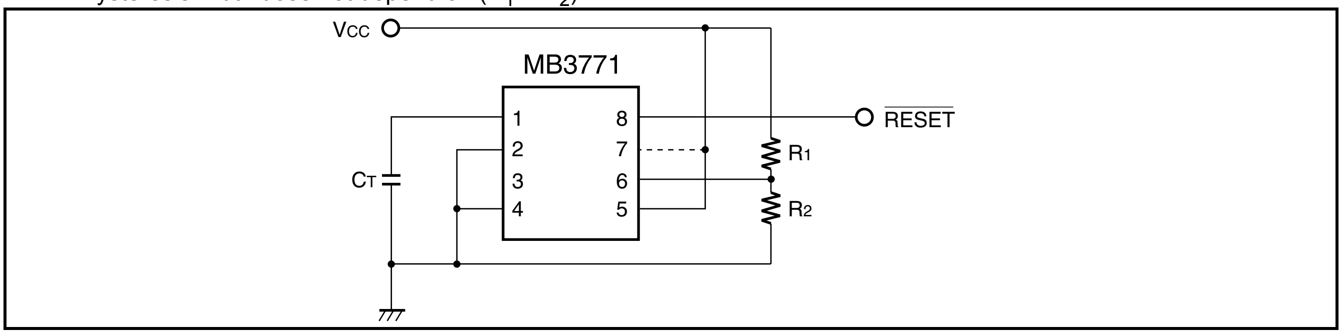


8.3 Arbitrary Voltage Supply Monitor

8.3.1 Case: VCC ≲ 18 V

- Detection Voltage can be set by R_1 and R_2.
  Detection Voltage = $(R_1 + R_2) \cdot V_{SB}/R_2$
- Connect Pin 7 to V_{CC} when V_{CC} less than 4.45 V.
- Pin 7 can be opened when V_{CC} greater than 4.45 V
  Power Dissipation can be reduced.

Note: Hysteresis of 28 mV at V_{SB} at termination is available.
Hysteresis width dose not depend on $(R_1 + R_2)$.........

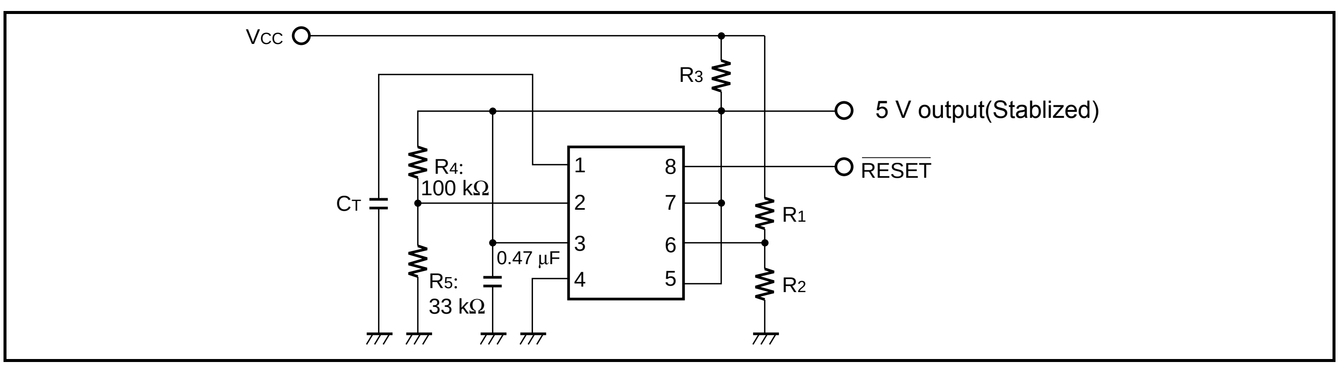


8.3.2 Monitoring VCC > 18 V

- Detection Voltage can be set by R_1 and R_2
  Detection Voltage = $(R_1 + R_2) \times V_{SB}/R_2$
- The $\overline{\text{RESET}}$ signal output is ≈ 0V (low level) and ≈ 5 V (high level). V_{CC} voltage cannot be output.
  Do not pull up RESET to V_{CC}.
- Changing the resistance ratio between R_4 and R_5 changes the constant voltage output, thereby changing the voltage of the high level RESET output. Note that the constant voltage output should not exceed 18 V.
- The 5 V output can be used as a power supply for control circuits with low current consumption.
- In setting the R_3 resistance level, caution should be given to the power consumption in the resistor. The table below lists sample resistance values for reference (using 1/4 Ω resistance).

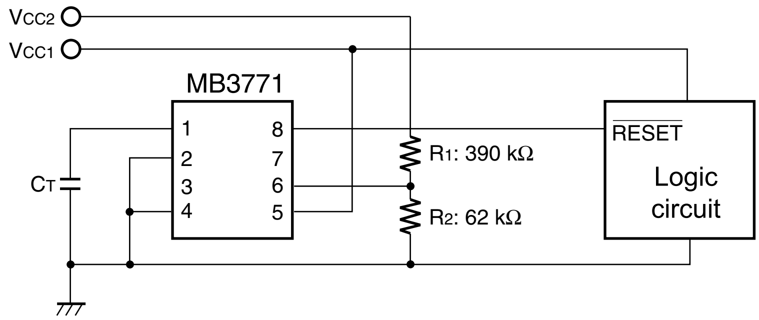
V_{CC} (V)	Detection voltage (V)	RESET Output min. power supply voltage (V)	R_1 (MΩ)	R_2 (kΩ)	R_3 (kΩ)	Output Current (mA)
140	100	6.7	1.6	20	110	< 0.2
100	81	3.8	1.3	20	56	< 0.5
40	33	1.4	0.51	20	11	< 1.6

- Values are actual measured values (using I_{OUTC} = 100 µA, V_{OLC} = 0.4 V). Lowering the resistance value of R_3 reduces the minimum supply voltage of the RESET output, but requires resistance with higher allowable loss.



8.4 5 V and 12 V Power Supply Monitor (2 types of power supply monitor V_{CC1} = 5 V, V_{CC2} =12 V)

- 5 V is monitored by V_{SA}. Detection voltage is about 4.2 V
- 12 V is monitored by V_{SB}. When R_1 = 390 kΩ and R_2 = 62 kΩ, Detection voltage is about 9.0 V.Generally the detection voltage is determined by the following equation.
  Detection Voltage = $(R_1 + R_2) \times V_{SB}/R_2$

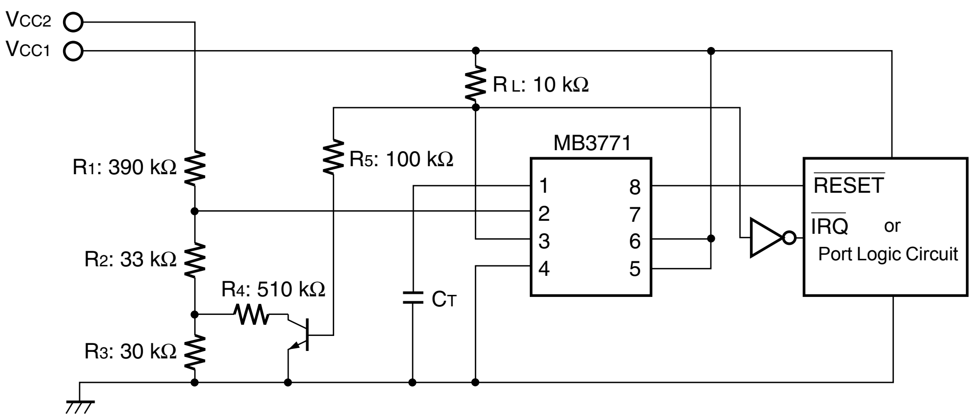


8.5 5 V and 12 V Power Supply Monitor ($\overline{\text{RESET}}$ signal is generated by 5 V, V_{CC1} = 5 V, V_{CC2} = 12 V)

- 5 V is monitored by V_{SA}, and generates $\overline{\text{RESET}}$ signal when VSA detects voltage sagging.
- 12 V is monitored by V_{SC}, and generates its detection signal at OUT_C.
- The detection voltage of 12 V monitoring and its hysteresis is determined by the following equations.

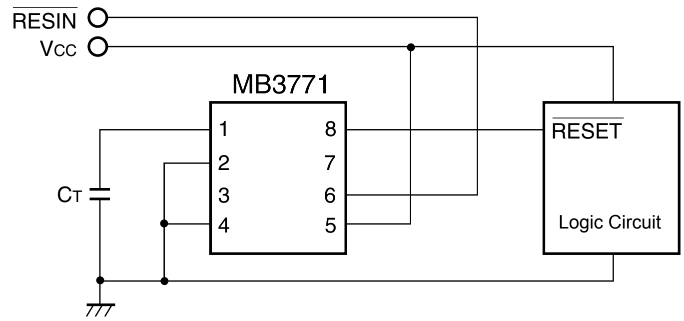
$$\text{Detection voltage} = \frac{R_1 + R_2 + R_3}{R_2 + R_3} \times V_{SC} \qquad \text{(8.95 V in the circuit above)}$$

$$\text{Hysteresis width} = \frac{R_1 (R_3 - R_3 // R_4)}{(R_2 + R_3)(R_2 + R_3 // R_4)} \times V_{SC} \qquad \text{(200 mV in the circuit above)}$$



8.6 5 V Power Supply Monitor with forced $\overline{\text{RESET}}$ input (V_{CC} = 5 V)

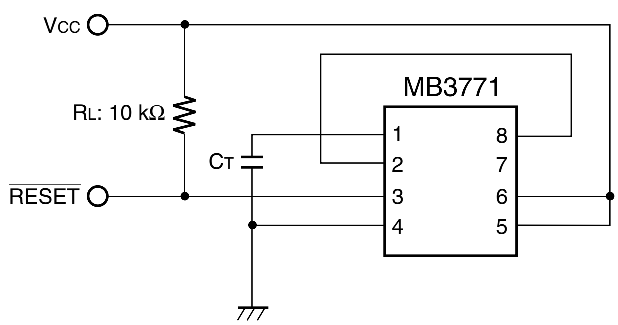
$\overline{\text{RESIN}}$ is an TTL compatible input.



8.7 5 V Power Supply Monitor with Non-inverted $\overline{\text{RESET}}$

In this case, Comparator C is used to invert $\overline{\text{RESET}}$ signal. OUTC is an open-collector output.

R_L is used an a pull-up resistor.

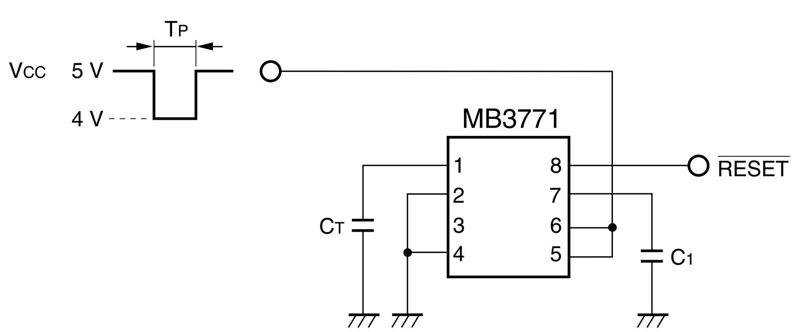


8.8 Supply Voltage Monitoring with Delayed Trigger

When the voltage shown in the diagram below is applied at V_{CC}, the minimum value of the input pulse width is increased to 40 µs (when C_1 = 1000 pF).

The formula for calculating the minimum value of the input pulse width [T_{PI}] is:

T_{PI} [µs] ≈ $4 \times 10^{-2} \times C_1$ [pF]



8.9 Dual (Positive/Negative) Power Supply Voltage Monitoring (V_{CC} = 5 V, V_{EE} = Negative Power Supply)

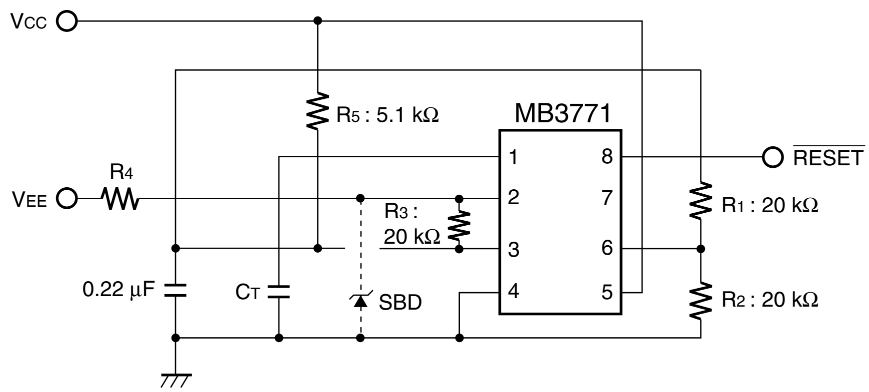
Monitors a 5 V and a negative (any given level) power supply. R_1, R_2, and R_3 should be the same value.

Detection Voltage = $V_{SB} - V_{SB} \times R_4/R_3$

Example if V_{EE} = −5 V, R_4 = 91 kΩ

Then the detected voltage = −4.37 V

In cases where V_{EE} may be output when V_{CC} is not output, it is necessary to use a Schottky barrier diode (SBD).



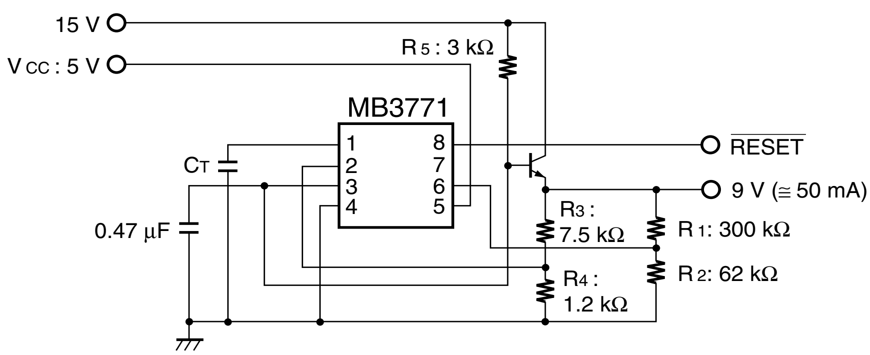
8.10 Reference Voltage Generation and Voltage Sagging Detection

8.10.1 9V Reference Voltage Generation and 5V/9V Monitoring

Detection Voltage = 7.2 V

In the above examples, the output voltage and the detection voltage are determined by the following equations:

Detection Voltage = $(R_1 + R_2) \times V_{SB}/R_2$

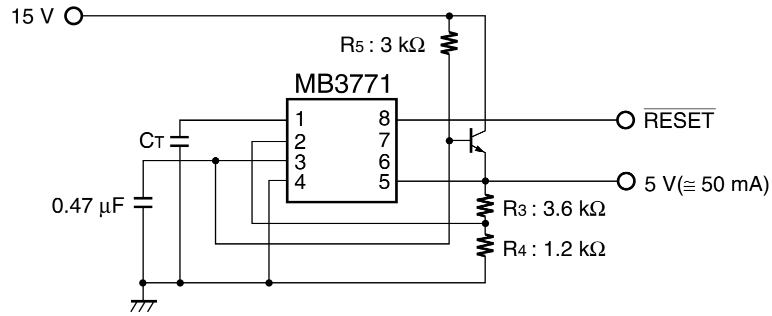


8.10.2 5 V Reference Voltage Generation and 5V Monitoring (No.1)

Detection Voltage = 4.2 V

In the above examples, the output voltage and the detection voltage are determined by the following equations:

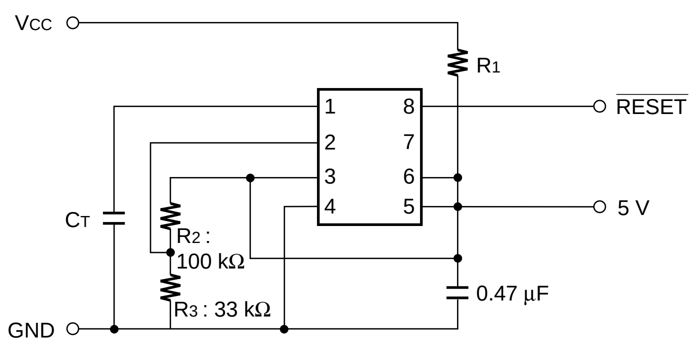
Output Voltage = $(R_3 + R_4) \times V_{SC}/R_4$



8.10.3 5 V Reference Voltage Generation and 5 V Monitoring (No. 2)

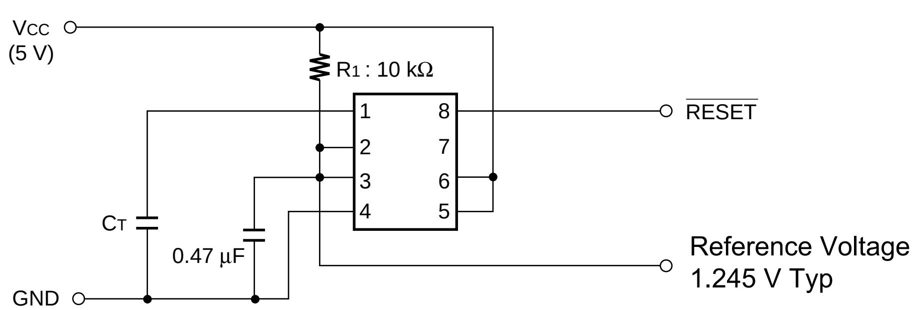
The value of R_1 should be calculated from the current consumption of the MB3771, the current flowing at R_2 and R_3, and the 5 V output current. The table below provides sample resistance values for reference.

V_{CC} (V)	R_1 (kΩ)	Output Current (mA)
40	11	< 1.6
24	6.2	< 1.4
15	4.7	< 0.6



8.10.4 1.245 V Reference Voltage Generation and 5 V Monitoring

Resistor R_1 determines Reference current. Using 1.2 kΩ as R_1, reference current is about 2 mA.

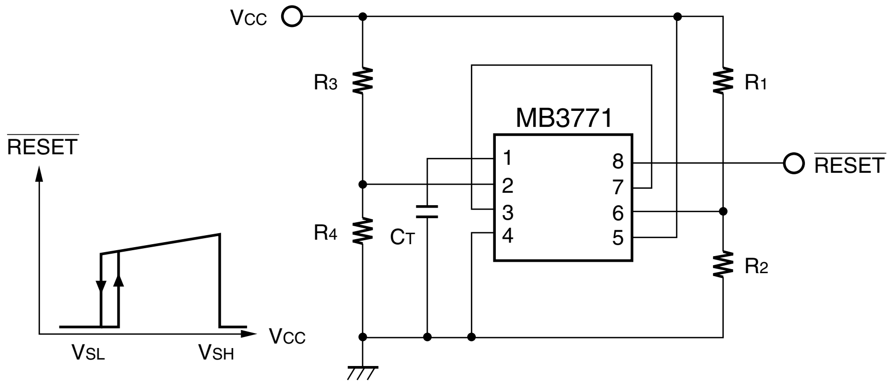


8.11 Low Voltage and Over Voltage Detection (V_{CC} = 5 V)

V_{SH} has no hysteresis. When over voltage is detected, $\overline{\text{RESET}}$ is held in the constant time as well as when low voltage is detected.

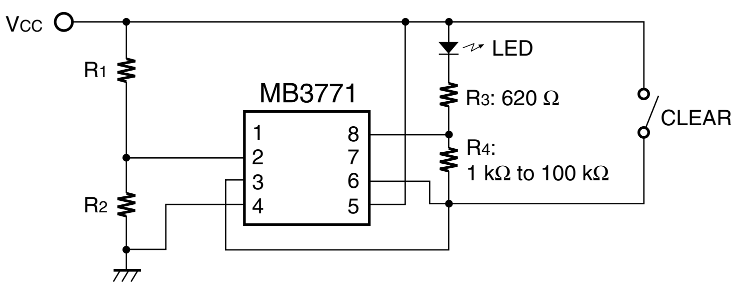
$V_{SL} = (R_1 + R_2) \times V_{SB}/R_2$

$V_{SH} = (R_3 + R_4) \times V_{SC}/R_4$



8.12 Detection of Abnormal State of Power Supply System (V_{CC} = 5 V)

- This Example circuit detects abnormal low/over voltage of power supply voltage and is indicated by LED indicator. LED is reset by the CLEAR key.
- The detection levels of low/over voltages are determined by V_{SA}, and R_1 and R_2 respectively.



8.13 Back-up Power Supply System (V_{CC} = 5 V)

- Use CMOS Logic and connect V_{DD} of CMOS logic with V_{CCO}.
- The back-up battery works after CS goes high as $V_2 < V_1$.
- During t_{PO}, memory access is prohibited.
- CS's threshold voltage V_1 is determined by the following equation:

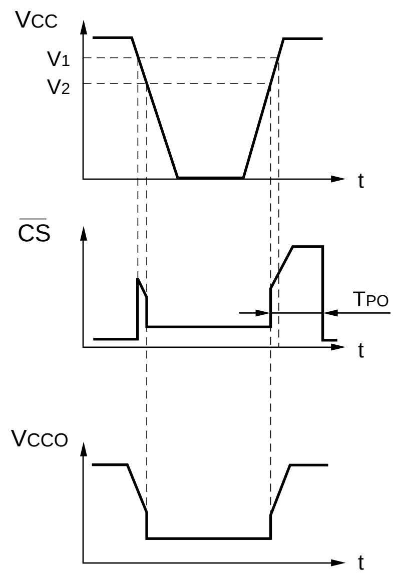
  $V_1 = V_F + (R_1 + R_2 + R_3) \times V_{SB}/R_3$

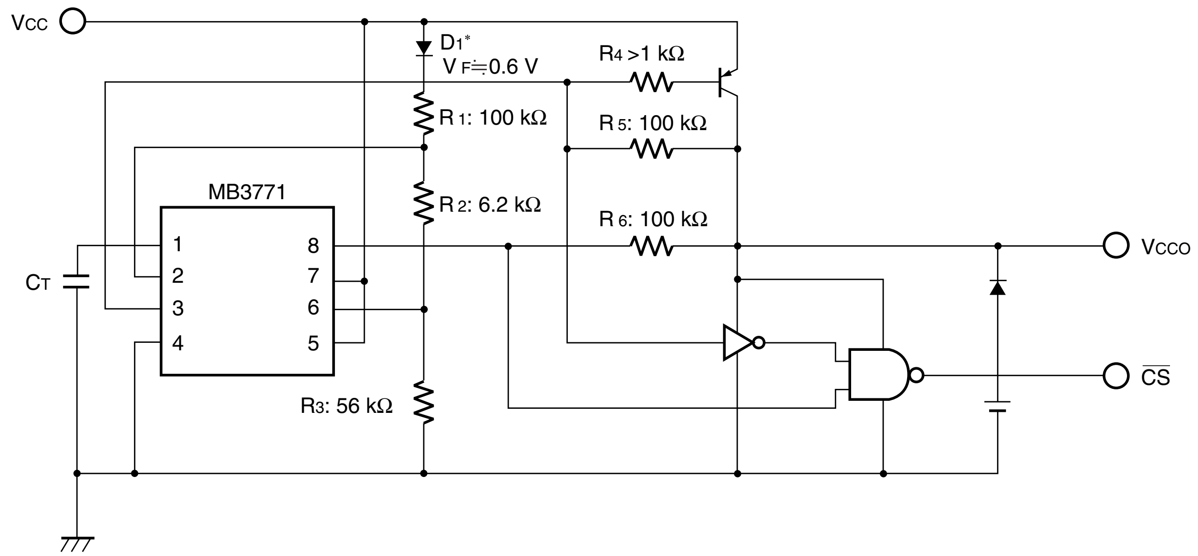
  When V_1 is 4.45 V or less, connect 7 pin with V_{CC}.

  When V_1 is 4.45 V or more, 7 pin can be used to open.
- The voltage to change V_2 is provided as the following equation:

  $V_2 = V_F + (R_1 + R_2 + R_3) \times V_{SC}/ (R_2 + R_3)$

  However, please set V_2 to 3.5 V or more.

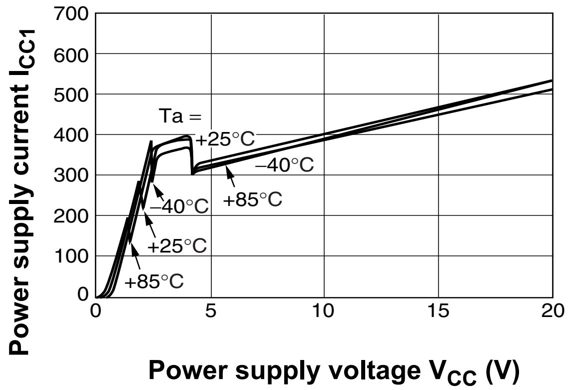




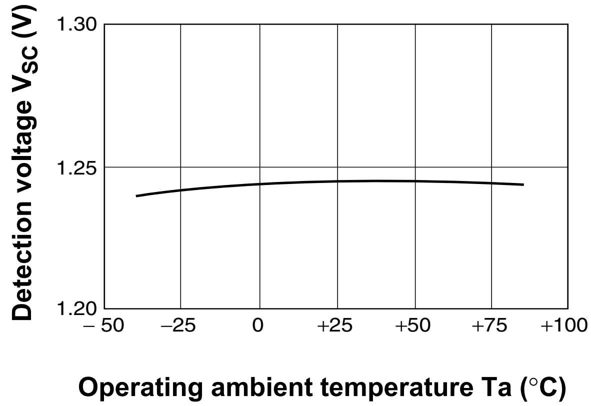
* : Diode has been added to prevent Comp.C from malfunctioning when V_{CC} voltage is low.
Set V_1 and V_2 with care given to V_F temperature characteristics (typically negative temperature characteristics).

9. Typical Characteristics

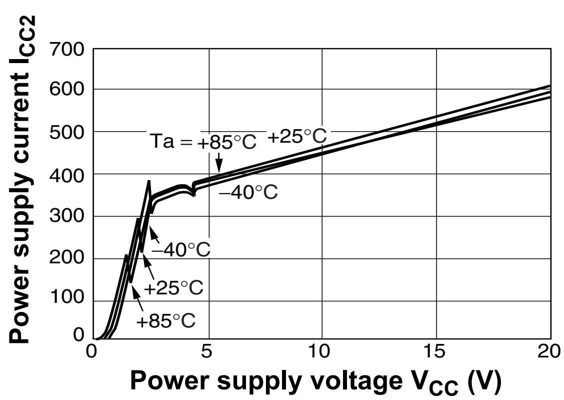
Power supply current (I_{CC1}) vs. power supply voltage



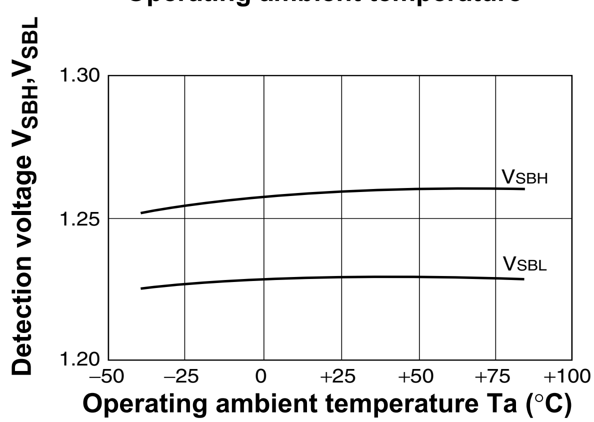
Detection voltage (V_{SC}) vs. Operating ambient temperature



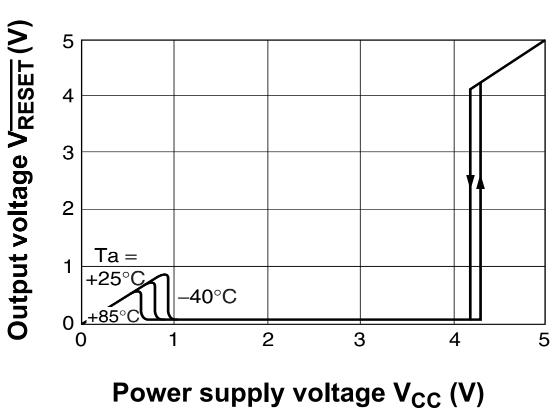
Power supply current (I_{CC2}) vs. power supply voltage



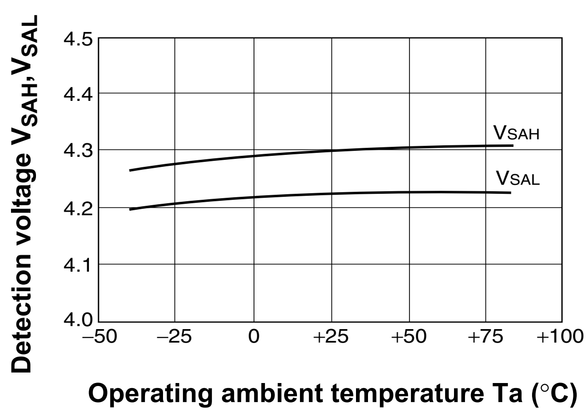
Detection voltage (V_{SB}) vs. Operating ambient temperature



Output voltage ($\overline{RESET}$) vs. power supply voltage



Detection voltage (V_{SA}) vs. Operating ambient temperature



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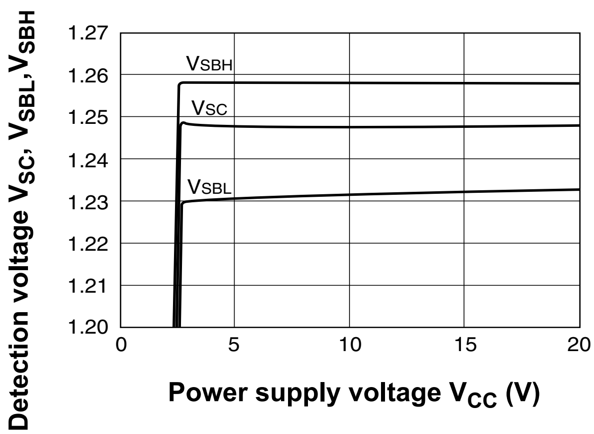
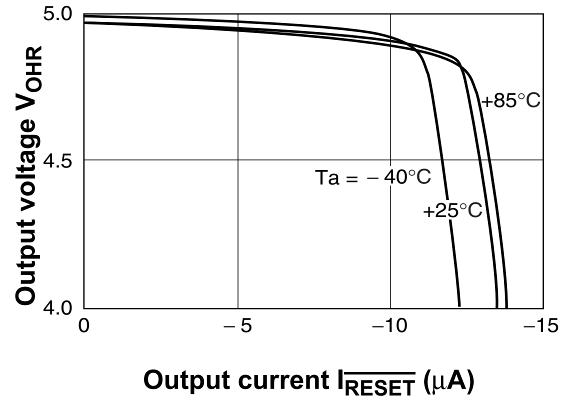
(Continued)

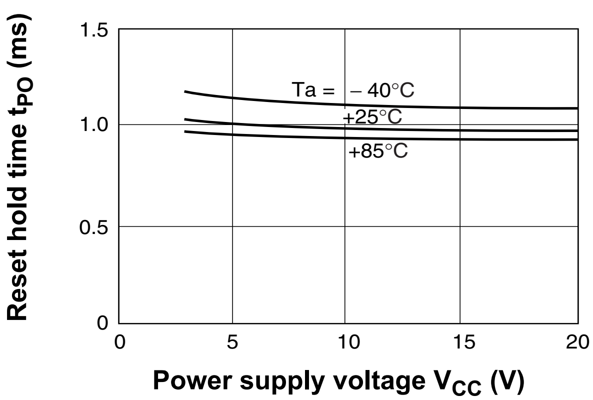
Detection voltage (V_{SB}, V_{SC}) vs. Power supply voltage



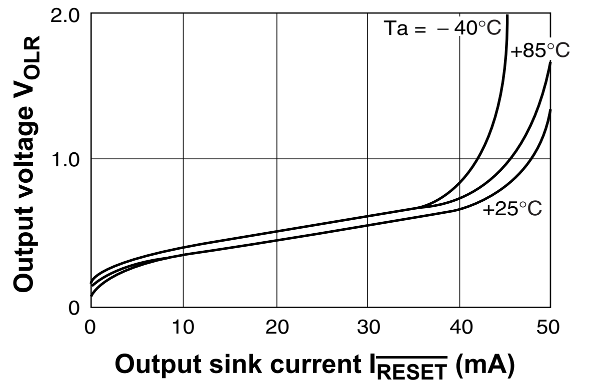
Output voltage (V_{OHR}) vs. output current



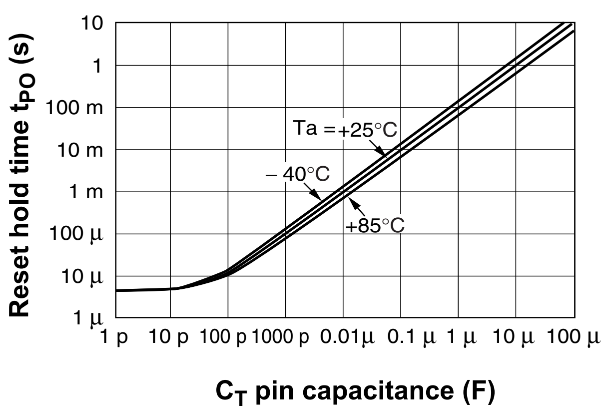
Reset hold time (t_{PO}) vs. power supply voltage (C_T = 0.01µF)



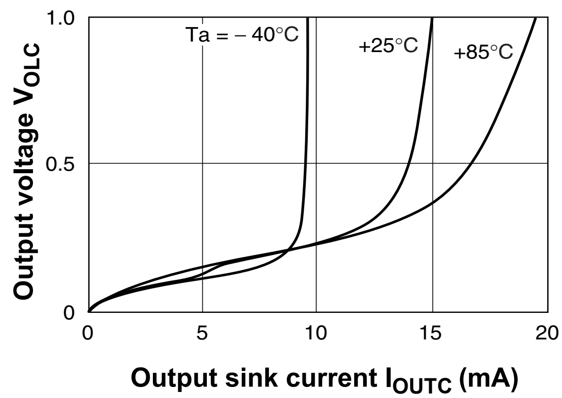
Output voltage (V_{OLR}) vs. output sink current



Reset hold time (t_{PO}) vs. C_T pin capacitance



Output voltage (V_{OLC}) vs. output sink current



10. Notes on Use

- Take account of common impedance when designing the earth line on a printed wiring board.
- Take measures against static electricity.
  - For semiconductors, use antistatic or conductive containers.
  - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  - The work table, tools and measuring instruments must be grounded.
  - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.
- Do not apply a negative voltage
  - Applying a negative voltage of −0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

11. Ordering Information

Part Number	Package	Remarks
MB3771PF-❑❑❑E1	8-pin Plastic SOP (SOE008)	–

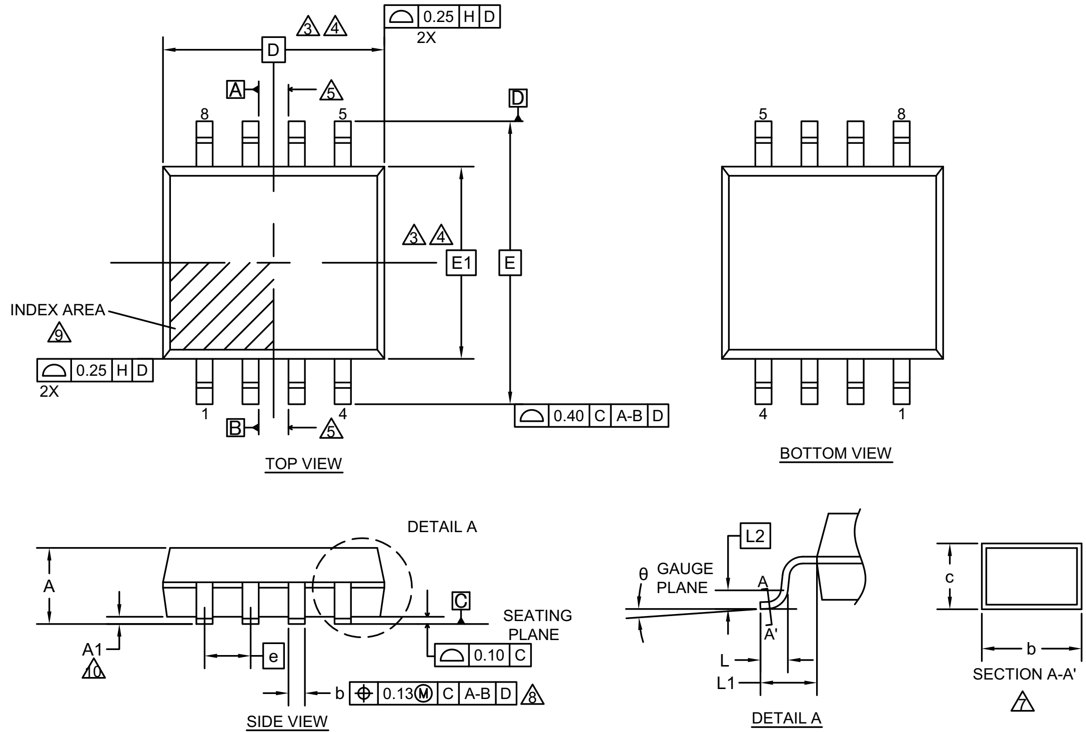
12. RoHS Compliance Information

The LSI products of Cypress with “E1” are compliant with RoHS Directive , and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE) .

The product that conforms to this standard is added “E1” at the end of the part number.

13. Package Dimensions

Package Code: SOE008



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	2.25
A1	0.05	—	0.20
D	6.35 BSC		
E	7.80 BSC		
E1	5.30 BSC		
θ	0°	—	8°
c	0.13	—	0.20
b	0.39	0.47	0.55
L	0.45	0.60	0.75
L1	1.25 REF		
L2	0.25 BSC		
e	1.27 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF : N/A

002-15857 Rev. **

Document History

Spansion Publication Number: DS04-27400-11Ea

Document Title: MB3771 Power Supply Monitor Document Number: 002-08511				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	TAOA	05/12/2006	Migrated to Cypress and assigned document number 002-08511. No change to document contents or format.
*A	5177314	TAOA	03/16/2016	Updated to Cypress format.
*B	5550024	HIXT	12/12/2016	Updated Pin Assignment: Change the package name from FPT-8P-M01 to SOE008 Updated Ordering Information: Change the package name from FPT-8P-M01 to SOE008 Updated Package Dimensions: Updated to Cypress format Deleted Marking Format (Lead Free version) Deleted Labeling Sample (Lead free version) Deleted MB3771PF-❑❑❑E1 Recommended Conditions of Moisture Sensitivity Level
*C	5606248	HIXT	01/31/2017	Deleted the part number, “MB3771PF-❑❑❑”, from Ordering Information Deleted the words in the Remarks, “Lead Free version”, from Ordering Information

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